Asia-Pacific Workshop on

FPGA Applications

Nanjing, China, 2013

Book of abstracts

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Asia-Pacific Workshop on FPGA Applications

Nanjing, China, 2013

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Workshop Preface

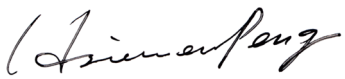
Welcome to the 2nd Asia-Pacific Workshop on FPGA Applications, held from November 1st to 3rd, 2013, at Southeast University, Nanjing, China.

The Asia-Pacific Workshop on FPGA Applications is the premier workshop in the Asia-Pacific region which brings together top talents in the field of FPGA design. In addition to the outstanding research papers presented and published in the Workshop. Award-winning projects from the 2013 InnovateAsia Design Competition will be also presented in the event where we see an increased number of participants from USA, China, United Kingdom, and Taiwan to share their design ideas. By promoting excellence in the programmable logic design, this workshop aims to further the knowledge and expertise through international awareness and mutual collaboration of the world's best engineering scholars in both academia and industry.

This year's conference brings together more than 200 professors, researchers, and students from over 50 different institutions. Hence, the conference provides for an international, cross-disciplinary, and multicultural platform for networking and developing new knowledge, connections, and long-term collaborations.

All workshop proceedings are included in the conference CD. For more information, please visit our website http://www.innovateasia.com for more details.

11 October 2013



Sean Peng
Chairman of Organizing Committee

Abstracts of
Outstanding Paper

Outstanding Paper

UK001

The BERIpad Tablet: Open-source Construction, CPU, OS and Applications

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We present a full desktop computer system on a portable FPGA tablet. We have designed BERI, a 64-bit MIPS R4000-style soft processor in Bluespec SystemVerilog. The processor is implemented in a system-on-chip on an Altera Stratix IV FPGA on a Terasic DE4 FPGA board that provides a full motherboard of peripherals. We run FreeBSD providing a multiuser UNIX-based OS with access to a full range of general purpose applications. We have a thorough test suite that verifies the processor in continuous integration. We have open-sourced the complete stack at beri-cpu.org including processor, systemon-chip, physical design and OS components. We relate some of our experiences of applying techniques from successful opensource software projects on the design of open-source hardware.

KEYWORDS Open-source, hardware, tablet, FPGA, Bluespec, BERI, MIPS, FreeBSD, Terasic, Altera

TW005

Fast Contrast Enhancement based on A Novel Dynamic Histogram Equalization Algorithm

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In this paper, a novel contrast enhancement algorithm based on the Histogram Equalization algorithm is presented. The proposed approach enhances image/video contrast without losing the original histogram characteristics. The algorithm is expected to process the video resolution efficiently but does not to overshoot the equalization with annoying side effects by using the difference information from the input histogram. The experimental results show that the proposed Dynamic Histogram Equalization (DHE) algorithm not only keeps the original histogram features but also enhances the contrast with much less computational efforts for large resolution. Furthermore, the proposed DHE algorithm can be easily applied to the FPGA hardware.

KEYWORDS Contrast Enhancement, Histogram Equalization, Dynamic Histogram Equalization, FPGA

Outstanding Paper

TW006

Design of Power Quality Recognition Platform

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In recent years, the Taiwanese government has been actively promoting industrial upgrading, as a result, most technology-oriented industries are benefiting a lot from this. However, poor power quality increases the power consumption and reduces the life expectancy of the equipment. Hence, power quality problems gradually arouse public attention.

In this thesis, an SOPC-based power quality analyzer (PQA) is designed. The main objectives of the proposed system are detecting transient voltage variations as well as analyzing the power harmonic interference. The transient voltage variation detection calculates the RMS value within a moving window length of half cycle. The harmonic analysis is performed with the application of Fast Fourier Transform (FFT) according to the requirements of IEC Std. 61000-4-7. The experimental results show that the proposed PQA is capable of detecting and capturing the power quality events.

KEYWORDS Power Quality, Transient Voltage Variations, Harmonic Analysis, Moving window, Fast Fourier Transform

TW011

Design and Implementation of Intelligent Desk Lamp

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In this paper, we proposed a FPGA based intelligent desk lamp system with a camera, two servo motors and LEDs. The proposed lamp can trace a moving book by automatic pan/tilt control. Thus, the user can read book with enough light for eye care. The architecture of the intelligent desk lamp system includes vision system and servo motors control system. The position data of the book can be obtained by the image processing module. According to the position data of the book, the pan and tilt angles of the desk lamp can be adjusted by two servo motors automatically. The adjustable ranges for pan/tilt are 60/30 degrees. The processing modules are implemented by hardware in FPGA. We use Verilog HDL to implement this system on Altera DE0-Nano kit with Cyclone® IV EP4CE22F17C6N FPGA.

KEYWORDS FPGA, Intelligent Desk Lamp, Image Processing, Servo Motor Control

Outstanding Paper

TW012

FairyTales – Fairly Detailed

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This document gives a detailed explanation about the design of our product and the implementation of it. The name of our product is FairyTales, which is a visual assistant with respect to some extending function such as taking photos and real-time handwriting. The functionalities of FairyTales are realized through DE2-115 board which is a powerful equipment designed for to create, implement, and test digital designs using programmable logic.

KEYWORDS FairyTales, auxiliary eyeglasses, augmented reality (AR), vision system, DE2-115, Innovate Asia, Altera

TW013

NeverFull

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In modern world, high-tech products are widely applied to all kinds of industries. However, in restaurants and bakeries it still requires a lot of human resource that costs a lot and is likely to make mistakes. NeverFull provides powerful functions to recognize different types of food. Shop owners can build the database easily by themselves to save a lot of time and effort.

KEYWORDS

Outstanding Paper

TW015

A Real-time Object Detecting and Tracking Design for Railroad Crossing Application

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As the promotion of transportation construction, there are a lot of railroad crossings in Taiwan. However, the traffic accidents are always happening on the railroad crossings every year. In order to protect the drivers against the accidents on the railroad crossing, an object detecting and tracking design is proposed for an automatic warning system. Since it is necessary to identify a vehicle getting stuck on the railroad crossing or not in a very short time, the very large scaled integration (VLSI) technique was used to develop the image processor for this system. This design not only detects any vehicle getting stuck on the railroad crossing or not but also tracks all vehicles across the railroad crossing. This double checking is guaranteed to the driver's life. This design was realized by hardware description language (HDL) verilog and realized by an Altera DE2-115a field programmable gate array (FPGA) development board. By using the VLSI technique, this design has the benefits of high performance, low cost, and low power consumption. The accuracy of vehicle detection can be greatly improved with the combination of object detecting and tracking techniques.

KEYWORDS Feature extraction, FPGA, object detection, object tracking, railroad crossing, VLSI

TW017

Vision-Based Robot Motion Control System by Using a SOPC System

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This thesis presents a SOPC-based servo motion control technique for the robot manipulator system. The system adopts MATLAB to perform image processing functions, such as the transformation of the color space, morphological operation, data classification of the object, the shape recognition and endpoint detection. For the servo motion control of the robotic system, it consists of two controller modules. The first one control module is consisted of quadrature encoder pulse circuits, limit switches detection, generation of pulse width modulation ,and point-to- point motion trajectory generator. Then, control signals are sent via FPGA to drive circuits for controlling each motor. The other module which includes a user interface and calculation of inverse kinematics, which is implemented via the NIOS II.

Finally, user can send commands via PC to perforem the shape recognition, data classification of the object's color, and play tic-tac-toe games on the basis of image processing. The experimental results have demonstrated the effectiveness and validity of the proposed FPGA system applied on the servo motion control of the robot manipulator system.

KEYWORDS SOPC, Arm Robot Motion Control, Image Processing

Outstanding Paper

TW018

Applying Dynamic Hair Dyeing Simulation On FPGA to Improve User Experience and Life Quality

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The purpose of this paper is to design a system avoiding user from getting unexpected hair dyeing result on FPGA DE2-115 which can perform real-time dyeing simulation.

In the system, user can have 55 default hair types, which have already been set in the devices, commonly used in hair salons. If there is a new hair color type that is not in those 55 defaults, the hair salon can adjust the value of red, blue, and green until the exact color result is obtained and then added to the system. The color information in RGB values will be showed on the LCD screen and the hair salon can easily change them only by a few ticks on the multi-touch board.

The system design architecture is consisted of three major parts. First, the camera collects the information and transports the data into the FPGA board. Second, the FPGA board processes and then an algorithm is applied to identify the correct region to be dyed. Also, in order to keep the hair texture, another algorithm is applied to imply for color scaling in the detected region. Finally, the multi-touch board displays the processing results and ready to receive user commands from the FPGA board.

The system provides a more efficient and precise way to simulate the dyeing results of user in real-time compared to the common method in dyeing hair by just using imagination based on category.

KEYWORDS Hair dyeing , FPGA ,Real-time, Hair detection , Color scaling

TW019

iCoach – Interactive Coaching System on Altera DE2-115 FPGA Architecture

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In this paper, we present a new interactive, 2-player coaching system – iCoach, based on Altera DE2-115 FPGA board. The coach can be the 2nd player or any video stream provided by the user. With beautiful virtual background image and different background music choices, he/she can enjoy exercising with the coach and get real-time scores and comments on the performance of their overall motion, thus improving their motor skills. Also, iCoach provides interactive motion games for users to have fun dancing and painting with body parts. In comparison with existing motor learning devises such as Wii Fit, iCoach is more flexible since it enables users to set up their own coaches and virtual environments. Moreover, iCoach is more computationally efficient and uses less memory due to the carefully designed algorithms and the arrangement of FPGA memory.

KEYWORDS FPGA, Dance, Coach, Motion-sensing, Interactive game, Rehabilitation

Outstanding Paper

TW021

FPGA Platform for Realtime 3D Reconstruction of Digital Holograms

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This paper present a novel FPGA-based hardware platform for realtime 3D reconstruction of digital holograms. The platform can be viewed as a hardware implementation of Fresnel transform for diffraction computation. The circuit employs a novel 2D FFT processor operating in fully pipelined fashion for accelerating the computation. Experimental results reveal that the proposed architecture has the advantages of high throughput, high accuracy and low power consumption for the 3D rendering and display.

KEYWORDS Holography, 3D Display, FPGA.

TW022

An Alternative Reading Eye for the Visual Impaired

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In this generation, everyone has the right to receive real-time and great amount of information. However, it is difficult for the visually impaired people to have the benefit of using this great information. In this paper, a reading system is proposed as an alternative eye for the visual impaired people. By this reading system, the information of words is transformed into the information of voice. It helps the visually impaired people to get all kinds of information quickly and easily. This system was developed based on the image processing technique, by which the captured image is converted into the text information by a character recognition technique. In order to achieve the demands of fast computing, multiple texts identification, huge database accessing, and real-time application, the very large scale integration (VLSI) technology was used to improve the performance of this system. This design was implemented by an Altera DE2-115a field programmable gate array (FPGA) board with a 5 Mega Pixel lens to capture the image of the book. For the future development, this system will be connected with the cloud systems, by which the recognized words can be translated into voice information by the cloud computing and tools. We hope this system can help the visually impaired people to get information from the books and papers independently.

KEYWORDS FPGA, image segmentation, image zooming, text detection, visual impaired people, VLSI, word identification

Outstanding Paper

TW028

SpeakING

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SpeakING is a good helper to those having troubles in singing–if you can Speak, you can SING. It is because SpeakING can transform normal speech into a melody you create. Moreover, SpeakING can be more entertaining when combined with specifically designed sound effects. This article will introduce the theorem and the circuit realization of SpeakING on FPGA board.

KEYWORDS vocoder, channel vocoder, voice changer, sing, pitch

TW031

Design An Omni-directional Mobile Platform with A Cannon

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In this thesis, we implement a remote-control cannon vehicle. There are three parts of system architecture within the cannon vehicle described. The first part is mechanical structure design. The second part is the remote controller design. The last part is the motor controller design. For the mechanical structure design, we use 3D CAD software to draw the sketch stress analysis, and to ensure the materials don't change shape. In the remote controller, a Nintendo Wii joystick is used to control the directions of the cannon vehicle. Finally, we separate the motor controllers into two parts. One part is the controller for the vehicle, and the other part is the motor controller for the cannon.

KEYWORDS mechanism design, remote control, motor control

Outstanding Paper

TW039

FPGA and Virtual Reality Based Minimally Invasive Surgery Training System

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The objective of this system is providing an effective tool for junior surgeons to practice and evaluate their fundamental skills and ability of minimally invasive surgery (MIS). In order to achieve these objectives, this system combines the technologies of FPGA and virtual reality (VR) to build a VR based MIS training system. The main function of FPGA is to provide a real time and precise 3D location of instrument. We use DE2-115 FPGA board as the main platform, two D5M cameras as the image sensor in the homemade surgery training box, and the stereo vision technology to get the instrument's 3D location. Then the FPGA platform sends instrument's 3D location to the 3D VR game on the PC in real time by the UART interface. The PC receives the instrument's position from the FPGA and its rotation information measured by the sensor module to control the visual objects in the game. The system can train user's hand-eye coordination and sense of space.

KEYWORDS Minimally invasive surgery, virtual reality, FPGA, surgery training system, stereo vision

Outstanding Paper

TW041

Based on Auto Comfortable Disparity Adjustment Real-Time 3-D Generation System

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This paper use colour image and its depth information to generate virtual images in different viewpoint. There is a distance sensor to detect the distance form viewer to displayer which is one of parameters for generating virtual images. The comfort of watching 3-D image could be enhanced by changing the parameters. All the system is implemented on FPGA.

KEYWORDS FPGA, DIBR, View distance, Watching comfort, Disparity adjustment

TW042

The Implementation of Triple-Disk-Failure Tolerant RAID

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A brand new algorithm of RAID for tolerating triple disk failures is presented in this paper. A prototyping system is built on Altera FPGA DE2-115 board. To build this system, the PC and FPGA board are integrated to perform as the system development platform to increase the visualization of details inside the system. Also, this platform is used to transfer the designs from the original simulation software into engineering system using HW and SW co-design concept. The advantage of this platform is that the developer can do the algorithm proof, component/module design, testing and system integration efficiently. In the future, such triple-failure recovery technique should be widely used in storage system, network and cloud computing.

KEYWORDS RAID, Fault-tolerance, HDD failure, FPGA, platform

TW046

Visual Surveillance System under Bad Weather Conditions

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This paper is focus on the development and implementation of algorithms under Bad Weather Conditions, including moving object detections, Automatic Brightness Correction, Shadow Removal, and Rain Removal. Moving object detection plays an important role in intelligent surveillance system. Although there are many people propose many different methods to detect moving objects, but also based on PC or embedded platforms to achieve it. If want to provide object detection, tracking and identification, always depend on a highly complex algorithms to make accurate judgments. So it would be difficult to achieve real time. This paper proposes an implementation base on FPGA and using Verilog HDL to design it. It achieves real-time monitoring purposes, and it can be applied to bad weather conditions. It is useful to exclude the external environment and improve detection of accuracy.

KEYWORDS bad weather conditions, brightness correction, moving object detection, surveillance system, FPGA

TW055

Portable Healthcare System with Low-power Wireless ECG and Heart Sounds Measurement

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In this paper, we design a portable healthcare system to establish a mobile telecare environment for modern people. The environment can save the resource for medical care and let patients feel like the doctors are always around them whenever and wherever they are. Our system provides remote monitoring of the ECG signals and heart sounds for both doctors and patients. We use the Altera's DE2-115 development platform and Android phone to develop a low-power and portable healthcare system. In our system, a wearable ECG recording prototype is developed to transmit ECG signals of users to the DE2-115 broad. In addition, the heart sounds of users from stethoscope can be the input signal of the broad. Then the FPGA is like a digital signal processor to analyze the ECG signals and heart sounds signals in order to detect RR intervals to get heart rate. The information of the signals of heart can be shown on the LCD touch screen on the DE2-115 broad so that the users can know about their physical condition immediately. At the same time, the signals data will be transmit to Android phone through the Bluetooth and then by 3G/WiFi services of Android phone transfers the recorded data to the medical cloud.

KEYWORDS electrocardiogram (ECG) measurement, heart sounds, phonocardiogram (PCG) measurement, telecare, digital signal processor, FPGA

Outstanding Paper

TW056

Adaptive Electric Pen for Virtual Reality Rehabilitation

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In this FPGA implementation, we aim to create a virtual-reality rehabilitation environment of adaptive electric pen so that the patients can be trained for their hand movement. The infrared ray (IR) is used to sense the location of the electric pen in the maze. With 8-bits serial analog-to-digital converter, the received signal strength corresponding to the distance between the obstacle (pen) and the IR sensor is translated into digital signals for FPGA to further process. The maze is configurable and projected onto the screen by the FPGA output signal to the VGA port. The patients/players can see the maze on the screen and control the electric pen moving in front of the screen to experience the virtual reality. Even the maze on the screen is large, only three IR sensors having a spacing of 2 cm are used, which are mounted on a base carried by a track. The track is driven by a stepping motor, whose control signal is sent from FPGA so that the position of the electric pen can be traced and be kept in the detection region of three IR sensors. With these designs, we can avoid using a lot of IR sensors that are placed around the peripheral sides of the maze and can also reduce power consumption. Hence, the size of the maze can be varied from simple to complex training phases without altering the number of IR sensors. Also, the fatigue state of the patients due to repetition of the same action can be improved. With injection of entertainment elements, the rehabilitation can be more interesting.

KEYWORDS Electric pen, Virtual reality, IR sensor, Kinect, Wii, Rehabilitation, FPGA

TW057

The Implementation of FPGA Platform for the Motion Control of A Two-Wheel Robot

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This research is trying to control a two-wheeled-driven inverted pendulum using a digital control system implemented by FPGA. This system can automatically be balanced upright driving by a closed loop negative-feedback control. This system integrates a gyroscope and an accelerometer to measure the tilt angular velocity and acceleration of the robot for more accurate motion control. A filter is applied by using sensor fusion technology; that is used to reduce noise caused by many factors. These modules are not only designed to calculate the correct tilt angle for system PID feedback control, but also interfaced by using SOPC design. Due to the use of multiple interfaces, real-time interaction, complicated modular control, and motion planning and controllers in hardware and software design process should have better visualization to support the analysis of the proportional-integral-derivative controller so that the concept of system platform is also applied. The system platform uses PC as the Host to view the messages through mobile system's data connection.

KEYWORDS FPGA, two-wheeled-driven, sensor fusion, PID, system platform, visualization

Outstanding Paper

Outstanding Paper

TW058

Intelligent Rubik's Cube Solver

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This paper is describes using an FPGA chip to solve a Rubik's Cube. A CMOS camera is used to sense the colours of Rubik's Cube. NXT motors and a Lego building blocks construct a hand-like mechanical structure to push and turn the Rubik's Cube. We build a SOPC system and a Nios II processor is used to recognise the colors of Rubik's Cube and calculate the resolving actions of Rubik's Cube.

KEYWORDS Rubik's Cube, Artificial Intelligence, FPGA, NXT.

TW059

FPGA Rapid Prototyping of NFC-TENS for Smartphone Healthcare

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With the Near Field Communication (NFC) capabilities, emerging smartphones can expand customized hardware in outside. However, the realization of such technology is still in its infancy. This paper proposes a prototyping technology of NFC tag protocol used for transcutaneous electrical nerve stimulation (TENS) converter for smartphones healthcare aids. The NFC-TENS design consists of four layer of ISO/IEC-14443A tag standard with a TENS realized in the application layer. One side of which is the wireless communication to NFC reader of smartphone and the other side the TENS pulse signal generation for massage. The implementation is based-on FPGA rapid prototyping technology combined with the Android system that supported for NFC standards. The results reveal that smartphones healthcare is feasibly improving the healthcare behavior while comparing with the traditional TENS.

KEYWORDS FPGA rapid prototyping, TENS, NFC tag protocol, smartphone healthcare, Manchester coding, Modified Miller coding, HW/SW co-design

Outstanding Paper

TW065

An Efficient Neuron-Based Camera Distortion Correction System

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This study proposes an efficient system architecture for camera distortion correction, in which a neuron-based camera distortion corrector (NCDC) is applied to rapidly correct various camera and lens distortions and manufacturing flaws in economical cameras. Compared to traditional camera models for correcting camera and lens distortions, for which more than two types of models are used, the NCDC uses one neural model to correct geometric distortions and asymmetric manufacturing defects.

The NCDC consists of a front-end that calculates back-map coordinates in distortion image space and a back-end that reads camera distortion image pixels from memory to interpolate a 24-bit color pixel corrected image. In a complex camera system with field-programmable gate array (FPGA), the back-end uses a burst mode and multi-port access architecture to fetch the image pixel from a high-latency memory, which increases the number of correction frames per second (CFPS) of the camera corrector. Moreover, a development board using high-speed memory was designed to increase the camera correction efficiency. The results show that the CFPS of an NCDC back-end with the proposed architecture is over 19.39x higher than professional solutions..

KEYWORDS back propagation, camera distortion, distortion correction, FPGA, geometric distortion, neural network

TW066

Want to Be A Maestro? A Simulation System Implemented on FPGA

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With a change of gesture, a conductor can control every division of the concert band in our system. By wearing a glove with infrared emitters in one hand, and holding the baton equipped with the ultrasonic transmitter in the other hand, the system is made to detect the changes of the gestures and the movement of the baton. Our two simple notions: an infrared emitting and receiving mechanism, and the Doppler effect. After sensing these stimuli, the system transmits these data to FPGA for analysis. The Musical Instrument Digital Interface (MIDI) processor then reads these analysed data, and modifies the speed and loudness of the music synchronously. Eventually, the music is played by the electric piano. By means of changed gestures, the conductor can alter the characteristics of music at his/her will, and hears the sound of modified music synchronously.

KEYWORDS Doppler effect, Infrared, MIDI , Conductor, Ultrasound

Outstanding Paper

CN003

Design and Implementation of Load-Balanced Multipath Self-routing Switching System

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In order to ensure high quality of service (QoS) for Next Generation Network (NGN), we construct a new Load-Balanced Multipath Self-routing Switching Structure which consists of the same two multipath self-routing fabrics. The result of simulation is inspiring for achieving 100% throughput and no delay or jitter. For this reason, we start on the implementation on an Altera StratixIV FPGA. And the whole FPGA system is designed into two collaborative components: the UDP system and the register system. With two algorithms around input and output two stages, incoming traffic is transformed into uniformity and then to their final destinations. During the later period debugging, software simulation platform and automated test platform are built, which contribute to our work very much. At last, we carry out several experiments to test and verify our system. The report of the test result accords with what we expected.

KEYWORDS Load-Balanced, Multipath Self-routing Switching Fabric, FPGA, UDP, Register

CN011

Design of Entropy Decoding Module in Dual-Mode Video Decoding Chip for H. 264 and AVS Based on SOPC

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This document introduces the hardware design of the entropy decoding module in dual-mode video decoding chip for H. 264 and AVS standard. The entropy decoding module designed in this document can realize the decoding of CA-2D-VLC for AVS standard and CAVLC and CABAC for H.264 standard. The Verilog HDL is used to accomplish RTL design and the FPGA implementation is achieved on an Altera Cyclone II EP2C35F672C6. The result indicates that the design efficiently reduces the circuit area and improves the speed of decoding.

KEYWORDS H.264, AVS, entropy decoding, FPGA, Verilog HDL

Outstanding Paper

CN014

Design and Implementation of DES IP Based on LEON3 SOPC

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This paper proposes a novel method to design and implement DES algorithm IP based on LEON3 SOPC platform. Since this DES IP core is a standard AMBA APB slave device, it can be easily embedded to SoC designs where AMBA bus is used as the interconnect interface, making it much more effective to implement DES algorithm in SoC designs. So comparing with common hardware implementation of DES algorithm, this DES IP core has a very large application prospects in SoC designs. Also the method this paper presents to design an AMBA APB slave device in LEON3 architecture can be referred to. The DES IP is simulated by Modelsim and tested within the LEON3 SOPC platform. Results indicate that this DES IP core has a fine performance and the method this paper demonstrates to design and implement an APB slave device is reliable and referable.

KEYWORDS DES, IP, LEON3, AMBA, SoC, SOPC

CN034

Intelligent Parking System Based on Nios II

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Intelligent parking system attracted increasing attention of the automobile manufactures in recent years. A reliable parking assistant system could reduce the rate of accident effectively and simplify the operation of the driver. This design takes Nios II as control core, uses camera to collect parking information, installs ultrasonic sensors to achieve ranging capabilities, adopts Ethernet port and wireless router to realize communication with Android smart phone and designs driver circuit to control car. The experiments show that this design can achieve real-time operation of the model car through smart phone to finish parking process. Meanwhile the car can complete parking automatically with the assistance of image and range information.

KEYWORDS Intelligent Parking, Nios II, FPGA, Android, Real time Image Processing

Outstanding Paper

CN039

An Eye Controlled System Based on Nios II

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In the background of current hot sight-tracking technology , this topic aims at designing an eye controlled system based on Nios II and solving the HMI problems of the disabled so that it can provide a way for them to communicate with the outside world, improve their ability of living and help them regain confidence. We have also designed some Interactive functions such as an eye controlled calculator, an eye controlled Whac-A-Mole game and an eye controlled voice-help. It can provide convenience and help them communicate with others, seek help, have fun and study.

KEYWORDS SOPC, VGA display, Image Processing, Relative Offset Calculation, View positioning; Edge detection

CN040

The Intelligent Detecting Robot

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With the current advanced SOPC technology carrier, intelligent detection robot system is designed. Using the DEII board of ALTERA company as the robot's control core, we realize the robot's navigation and positioning, environmental information detection and the function of information transmission. Detection robot system transmits the position and spot environmental information to the PC monitor, this can help operators to judge the scene of the accident situation for effective rescue work.

KEYWORDS Detecting robot, FPGA, DEII, GPS, EC

Outstanding Paper

CN050

Towards Wearable Virtual Reality System Using Micro IMU Controller and FPGA Platform

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Virtual Reality (VR) is a computer-simulated environment that can simulate physical presence in places in the real world or imaginary world. We use FPGA to implement this design to take advantage of its hardware/software co-design and its high computation speed. We use IMU as the main input. It captures and sends motion data to FPGA. FPGA plays an important role in this system. It drives hardware, processes data, and stores and manages pre-stored image or sound material. After processing, system outputs image and voice, and imports into media glass and speaker, which are used as output devices, respectively. The final result shows that our system designed with FPGA can run fast and smoothly, easy to maintain and update, and it shows great potential.

KEYWORDS

FPGA, co-design, virtual reality, sensor, media glasses.

CN051

Galaxian Game on Altera DE2-115 FPGA Architecture

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With the development of computer and network technology, the pace of people’s life is much faster. At the same time, the need for entertainment is also growing. The game based on handheld devices is becoming more and more popular. It has been booming along due to its educational, fun, casual, easy to carry, easy to operate, highly interactive and many other features to meet the people's entertainment needs. This paper introduces the embedded systems based on general-purpose software development model and development process, including the design of hardware platform and software. The design of the hardware platform is based on the Altera's DE2-115 Series development board, the software platform is Nios II EDS 10.1 and the programming language is C and VHDL. Based on the SOPC tool, we designed the reconfigurable IP cores of the VGA display, LTM touch screen. With Galaxian game as an example, we design a embedded game based on GUI. The results show that the game system is human-computer interaction friendly and it has quick response and action. This configurable IP core has high flexibility, variability, plasticity and it can achieve more functional expansion and development with the same resource.

KEYWORDS

Configurable IP core, DE2-115, FPGA, SOPC, hardware/software co-design

Outstanding Paper

CN053

Implementation of Music Broadcast System Using Altera DE2 Boards and Qt

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This paper will introduce a music broadcast system based on schedule using Altera DE2 boards and Qt technology. The system has Client/Server architecture. Qt technology is used to set up a server in Ubuntu operation system. It will manage all online DE2 boards and send commands to them to play music stored on SD card inserted into the board.

KEYWORDS FPGA, Scheduled Music Broadcast, Qt, Nios II

CN058

Intelligent License Plate Positioning Identification System Based on FPGA

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With the rapid development of China's national economy, intelligent transportation systems has become the main direction of the development of traffic management, and license plate recognition system technology as the core of intelligent transportation system plays a pivotal role. This paper describes a theory based on Altera's CYCLONE II EP2C35 devices on the platform location and license plate recognition system. The system mainly works like this: First, camera module reads a license plate image, then through the image plate rough positioning, image graying, median filter, sobel operator edge detection, image binarization, plate processing such as automatic positioning precision positioning plate, and also through the establishment of NIOS II soft-core processor for the license plate character segmentation, and then match a single character segmentation, license plate recognition. In this system, some of the basic positioning using Verilog hardware description language, implemented in hardware for parallel processing large amounts of data, processing speed, high accuracy. For image positioning plate, color image based positioning methods; the algorithm is simple, less memory, which makes it possible to achieve fast and accurate positioning plate. License plate segmentation algorithm uses the traditional template matching algorithm. By establishing SOPC system allows users more easily to interact through the software license plate recognition, thereby provides greater flexibility.

KEYWORDS license plate positioning, FPGA, the image processing, Character segmentation

CN059

Modified Visual Target Tracking Algorithm and Its FPGA Implementation

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Visual target tracking is the key problem in intelligent video processing. CamShift and Particle Filtering are classic and effective in visual target tracking algorithms, but they both need to analyse a large amount of probability statistic, leading to high algorithm complexity and low calculation efficiency. FPGA provides a competitive alternative for hardware acceleration to these applications. In this paper, we modify CamShift and Particle Filtering algorithms and propose a FPGA-based hardware accelerating architecture. Experiments show the embedded architectures have good performance and the Particle Filtering algorithm shows better robustness and real-time performance.

KEYWORDS target tracking, CamShift, Particle Filtering, FPGA, embedded system

Outstanding Paper

CN060

A Lane Departure Warning System Based on Monocular Vision

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This paper introduces a monocular-vision-based lane departure warning system. Based on a fast lane departure warning robust algorithm and the NIOS II of Cyclone IIFPGA as the core processor, this system can achieve the lane line detection effectively. The software and the hardware of the system are designed with the aid of the Avalon bus for customizing the IP core. Test results illustrate that both the accuracy and real-time performance of this system satisfy the demand of all-weather lane departure warning, and thus enable safe driving.

KEYWORDS lane departure, FPGA, lane line detection, monocular-vision

CN063

Intelligently-Controlled Quadrocopter with Autonomous Navigation using Android

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A quadrocopter is a new kind of unmanned aircraft that has the advantages of novel structure and excellent performance, relating to high, exact and sophisticated technology in many fields. It is of value to practical applications. At first, our team studied a quadrocopter's structure characteristics, attitude algorithm and flight control principle. Then a flight control system was designed which uses LB0 (LB0 employs EP3C10E144C8 of Altera Cyclone III as core device) and MPU-6050 as core device and inertial measurement device respectively. The system analyzes the control signal which android mobile phone sends by WIFI, fuses current sensor measurement data, estimates the aircraft's motion attitude and then calculates the motors adjustments. According to the motors adjustments, the system controls the motors to regulate the quadrocopter's flight attitude. It results in a good effect that Euler angles method and Kalman filtering algorithms are adopted to describe and calculate the attitude respectively. At the same time, the data from GPS module is transmitted back to android mobile phone by WIFI and then it helps the system realize autonomous navigation.

KEYWORDS Quadrocopter, Android, Intelligent Control, Autonomous Navigation, FPGA.

Outstanding Paper

CN064

Automatic Video Security System based on Face-Recognition and Wireless Communication

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A new kind of automatic video security system based on face-recognition & wireless communication is introduced in this article, including its design method, hardware and software architecture, and its operation results. In this system, the face images captured by the camera will be compared with the criminal face images in the original database, and the similarities between the two faces will be counted. If the similarity is higher than the threshold, an alarm signal will be sent out. The system consists of two parts. The first part is based on FPGA, which includes DE2-70 board offered by Altera corp. and peripherals such as analogical camera & CDMA Modem, etc. First, amount the hardware architecture, modules described by Verilog HDL and SOPC, within which Nios-II processor has been added, are built. Second, amount the software architecture, software is described by C/C++, a μC/OS-II is transplanted & customized tasks have been set. The function of part 1 are face-detection, face image interception, JPEG encoding & MMS (enveloping the JPEG face image) transmission. As to the second part, it is based on the PC program described by C/C++. The only peripheral in this part is another CDMA modem. The function of part 2 are MMS reception, JPEG files extraction & face-recognition (PCA). The system makes use of the advantages of FPGA, such as high operating speed, high integrated level & great convenience, etc. It also makes use of the existing wireless communication network & the PC which is highly efFigient in calculation, compared to FPGA. Therefore, a possible pattern of FPGA—remote wireless communication–PC combined system for video surveillance & intelligent modes-recognition have been introduced.

KEYWORDS FPGA, DE2-70, Nios-II, SOPC, Altera, μC/OS-II, face-recognition, PCA, CDMA, MMS

CN068

Multi-channel Radio Spectrum Monitoring System

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As the radio signal has a large range bandwidth and is complicated, here a digital multi-channel monitoring system is designed. The system tunes the frequency of wide bandwidth radio signal via controlling the RF terminal, processing the baseband data by a variable bandwidth digital down conversion, finally, applying the digital processing algorithm to obtain the spectral information. Here four scan modes are designed to monitor the radio signal effectively from different angles. The software radio technology is applied so that the system can update efficiently without changing the hardware architecture. Finally, the spectrum processing result is demonstrated in the software.

KEYWORDS Radio signal monitoring system, Software radio technology, Variable bandwidth digital down conversion, RF terminal, Multi-channel, Spectrum processing

Outstanding Paper

CN069

A Fisheye Lens 360 Degree Panoramic Monitoring System Based on the FPGA

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This paper designs and implements a panoramic monitoring system based on the FPGA fisheye lens. Fisheye images produced suffer from severe distortion. Therefore, it must be corrected to approximately rectilinear versions. Nowadays, most of the algorithms used to correct the fisheyes distortion are realized by software. In this paper, we compared three algorithms used for panoramic monitoring system. And the obtained result of the spherical perspective projection algorithm is promising. The spherical perspective projection algorithm is implemented on a FPGA and a panoramic monitoring has been achieved in a SOPC system.

KEYWORDS FPGA, panoramic monitoring, fisheye, spherical perspective projection, SOPC

CN072

3D Scanning and Modeling System Based on FPGA

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3D scanning is an important technology for today's 3D applications, especially when a universal model of a real-world object is needed. Laser scanning techniques are developed, but it is difficult for it to be common used because of their complexity and high costs. A 3D scanning and modeling system with non-contact passive techniques is presented in this paper. The system is based on Altera's Cyclone II FPGA, and by using the SOPC tools, components related to the system are integrated on the FPGA chip. We came up with image processing and modeling algorithms that are very suitable for FPGA, and made a simulation in MATLAB, the algorithms turn out to be fast and robust. And the paper shows the concrete architecture of our design. The system is cheap, simple in structure, highly integrated, relatively independent, and can make 3D models in .STL form.

KEYWORDS 3D, scanning, modeling, FPGA, MATLAB, SOPC, image processing

CN099

An Intelligent Reader Based on Nios II

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With the rapid development of Human-Computer interaction techniques, the hand is no longer the only input means of human physique structure. This paper describes an intelligent reader system, which based on head movements for the man-machine interface, realizes the operations like zooming, page-turning and row-scrolling on the reading interface, through the rough face detection and localization of facial feature points to achieve the tack and recognition of head movements.

KEYWORDS face detection, facial complexion model, facial feature points positioning, head motion identification, FPGA, SOPC, Nios II

CN100

Design of PET Bottle Cap Defect Online Detection System Based on FPGA

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This paper designed an online detection system based on FPGA, which was used to detect if there is defect in the internal and external ring of the PET bottle cap and stains in the steal of the bottle cap. Based on the hardware platform whose core processor is EP4CE115F29, taking advantage of the parallelism and pipeline of the FPGA ,this system detect the internal ring, external ring and the steal of the bottle cap , then make a judgement. The MegaWizard module named Median Filter was used to smooth the image and threshold value segmentation was used to extract the part in which we are interested, and then judge whether there is stain in it. We used the projection of the gray level to get the center of the bottle cap, and then comparing with the center gravity to judge if the bottle cap is qualified. What is more, the edge detection arithmetic named Scharr was used to calculate the circular degree of internal ring, then judge if there is a defect. By experimenting repetitively, the arithmetic is useful that the system can detect the PET bottle cap efficiently. The number of the bottle cap detected the bottle is more than 50000, and the detection precision is 3.

KEYWORDS PET bottle cap, defect detection, smooth process, threshold value segmentation, edge detection

Outstanding Paper

CN107

Design and Implementation of Nios II-based LCD Touch Panel Application System

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This paper explains a system design for developing LCD touch panel applications by means of embedded system approach. Two Avalon-compatible IPs, acting as the LCD-display controller and the touch panel ADC controller are designed respectively for Nios II-centered SOPC. To verify the design, a game software named Lianliankan is developed on a SOPC containing the two custom IPs. The result indicates that the design has good usability, and satisfies the demand of application development better.

KEYWORDS touch panel, Intellectual Property, Nios II, Avalon, system-on-a-programmable-chip (SOPC)

CN122

The Permanent Magnet Synchronous Motor Vector Control System Based on FPGA

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In this paper, an FPGA chip and the external circuit is to achieve permanent magnet synchronous motor vector control system. Using Altera's Cyclone III EP3C25Q240C8N, rich programmable logic on-chip resources are utilized to realize the vector control of the system. Moreover, the right circuit of sampling and conditioning is the key point to the reliability of Closed-loop system. Finally, the experimental results show that Speed can follow the instruction and closed-loop system is reliable.

KEYWORDS FPGA, Vector control, Closed-loop system

CN141

The Production and Research for Humanoid Robot

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Humanoid robot that has always been a dream for humankind to develop has the external behavior of human beings, human intelligence and flexibility, the ability to communicate with people and constantly adapt to the environment. It is humanoid robot that is designed to imitate.

The morphology and behaviour are from human. Generally, it has the humanoid limbs and head. We have produced the humanoid robot by CAD software and designed the robot's structures according to human. The control panel consists of Cyclone II and MSP430.It can be achieved to control the robot dancing movements by comprehensive programming.

KEYWORDS simulation, communicate, Msp430, comprehensive, humanoid robot

CN147

Music Synthesizer Designed on FPGA

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As touch technology has become a hot spot of human-computer interaction in recent years, we accomplished the design--Music Synthesizer on LCD touch screen. We took use of the resources from board DE2-115, combined with Verilog HDL and C Language under the environment of Quartus II and Nios II Eclipse of Altera's. In the time when digital music develops in such a high speed, our design can achieve four different kinds of instruments playing and the control of changing the timbre, making more people able to create music themselves under a lower cost.

KEYWORDS music synthesizer, FPGA design, timbre, SOPC Builder, Nios II

Outstanding Paper

CN152

Design of A Six-stage Pipelined MIPS Processor Based on FPGA

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We design a 32-bit embedded six-stage pipelined processor which is compatible with MIPS instruction set. The six stages make the task of each stage balanced. We use forwarding and stalling to solve data hazards. Control hazards are solved by predicting which instruction should be fetched and when the pipeline will be flushed if the prediction is later determined to be wrong. The processor is implemented in DE2 development board, and its operating clock frequency can be up to 81.7MHz. In the end we present the comprehensive results of the design. Besides, we show the software simulation and hardware verification to prove the correctness of the design.

KEYWORDS MIPS, embedded, pipelined processor, hazards, FPGA

CN156

Embedded Test Technology of Switching Power Supply Based on FPGA

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In this paper, an embedded test technology of switching power supply based on FPGA was introduced to solve the shortcomings exist in the traditional detection methods, such as the complex process of maual detection, long test time, maintenance and support difficult, high cost of maintenance, etc. The FPGA implementation has been achieved on the Cyclone EP2C35F672C6. The results show that it can realize the automatic detection of switching power supply, improve the fault detectionrate and isolation rate of switching power supply, shorten the test time, reduce the test difficulty, improve the life cycle of switching power supply, reduce the life cycle cost of switching power supply, and this equipment is feasible and versatile.

KEYWORDS FPGA, Switching Power Supply, Embedded Test Technology

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