Design of Power Quality Recognition Platform

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Abstract— **In recent years, the Taiwanese government has been actively promoting industrial upgrading, as a result, most technology-oriented industries are benefiting a lot from this. However, poor power quality increases the power consumption and reduces the life expectancy of the equipment. Hence, power quality problems gradually arouse public attention.**
In this thesis, an SOPC-based power quality analyzer (PQA) is designed. The main objectives of the proposed system are detecting transient voltage variations as well as analyzing the power harmonic interference. The transient voltage variation detection calculates the RMS value within a moving window length of half cycle. The harmonic analysis is performed with the application of Fast Fourier Transform (FFT) according to the requirements of IEC Std. 61000-4-7. The experimental results show that the proposed PQA is capable of detecting and capturing the power quality events.

Keywords— **Power Quality; Transient Voltage Variations; Harmonic Analysis; Moving window; Fast Fourier Transform**

I. INTRODUCTION

In the past few years, the active promotion of industrial upgrading by the Taiwanese government has led to the flourishing of many high tech industries. In fields such as communications, medical, manufacturing, and financial transactions where the dependence of electronic equipment has grown stronger and stronger, people have been invested more and more resources, hoping to effectively improve work efficiency and improve product quality. However, the power consumption rate and the life expectancy are closely related to the quality of the power supplied. Therefore, the qualities of power have been taken more and more seriously.

Some common power quality problems are one, voltage transients caused by adjacent feeders struck by lightning, short circuit. Two, electric harmonic pollution caused by non-linear loads such as power electric conversion. Third, voltage flicker caused by rapid changes in load, such as arc furnaces in operation. These unregulated power supplies often cause electronic devices to malfunction. One can imagine that the production system will result in plant downtime or equipment damage and other serious accidents; in the financial market place, it will cause transaction failure or system errors and other serious losses; on other occasions, it could even be harmful to people's lives. Therefore, power quality monitoring and improvement is currently a very important issue.

A detailed description and classification of power quality events, including abnormal changes in voltage, power harmonic interference and phase imbalance can be found in IEEE Std. 1159-2009 [1]. In recent years, because of the rapid development of power electronics, power electronics converters and other widely used nonlinear loads, the harmonic interference has been much more rampant, many advanced countries have thus developed harmonic emission standards to meet the power supply terminal and terminal requirements. Given the requirements for power quality, the development of high-precision power quality monitoring equipment to carry out long-term monitoring is definitely necessary.

II. LITERATURE REVIEW

Many domestic and foreign experts and scholars in the past have done a great deal of research on power quality problems. The research is divided into two parts, the detection and analysis, and maintenance and improvement of power quality. This article will focus on the detection and analysis of power quality.

There are many ways to detect and analyse power quality, the most straightforward approach is to design algorithms base on the characteristics of the original waveform in the time domain, such as the envelope waveform detection method, the slope of the waveform detection method, the zero frequency detection method, etc. These algorithms will be affected by signal frequency, noise or signal interruption, leading to an error detection. Therefore, while calculating in the time domain, it is common to adopt the RMS (Root Mean Square, RMS) as a measure of power quality. As in [2] that the RMS value was used to classify the type of voltage event. But RMS computing may create effects similar to smoothing filter, and it cannot detect signal surges or transient changes. Another approach is to be analysed in the frequency domain, usually in the Fourier transform, wavelet transform and other ways to detect in the time domain where signal characteristics cannot be observed.

There are also a lot of literature in recent years talk about combining these methods and artificial intelligence, such as the Back-Propagation Neural Network, (BPNN) [3], probability neural network (PNN) [4] and adaptive linear Artificial Neural Network (ADALINE) [5], etc. In some implementations, the current literature adopts mostly DSP [3] [6] and FPGA [7] [8] for systems development, as well as a small part on a personal computer using LabVIEW virtual instrument design [5].

III. Power Quality Analysis

This chapter describes the system used by the power analysis techniques and explains some technical details. The details include a discussion of the impact of even harmonics method on calculating mobile Windows and the limitations and effect of Fast Fourier Transform.

A. Transient voltage change detection

Transient voltage change detection method is based on a comparison of RMS voltage and the set threshold to determine whether the occurrence of voltage dips, swells or interrupts. The more frequent the comparison is, the more easily it is to immediately detect abnormal events. The system was conducted in a way that a sample is collected after each comparison, thus the valid value will be calculated after each point. To simplify the design, it uses moving window RMS to calculate the valid values. Mobile window calculation refers to a fixed length calculated by the sampling points. In each new sample point comes after the removal of the oldest sample point, so the overall calculated length is fixed, as is the same as moving a window is calculated. Moves shown in Figure 1, each window contains N sample points. The results shown below in Figure 1, can be observed in the case of a change in the RMS voltage of the variations.

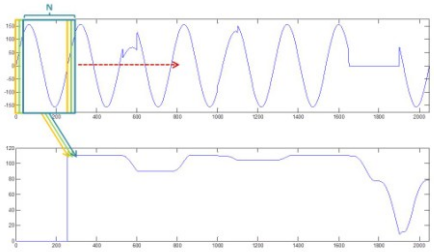

Fig. 1 Schematic moving window RMS calculation

In actual applications, the fact that the window size can be set to a half cycle is because an ideal AC power has a symmetric positive and negative half-cycle. Therefore, a half cycle rms value of the signal can also show the effective energy completely. Half-cycle RMS Windows computing makes the calculating and the detection of any voltage anomaly easier and faster. Shown in Figure 2, it can be observed that in the half-cycle RMS calculation window, it is much more rapid than it is over a whole cycle.

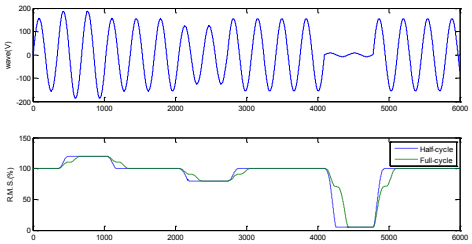

Fig. 2 half cycle and a cycle moving window RMS calculation results of the comparison

B. Discuss the influence of even harmonics

Half-cycle RMS calculation is based on the assumption that the signal is a symmetric positive and negative half-cycle sine wave signal, but when the signal contains harmonic components, it will cause the signal to no longer have the positive and negative half-cycle symmetry in nature. This prevents the half-cycle RMS calculation from fully presenting effective energy signals, creating various sizes of even harmonics and thus cause different degrees of error. Figure 3 the figure contains 20 percent of the second harmonic sinusoidal signals, Figure 3 below shows the semi-period moving window RMS calculation, the results can be observed in the nominal value of 81.86 - 115.5%.

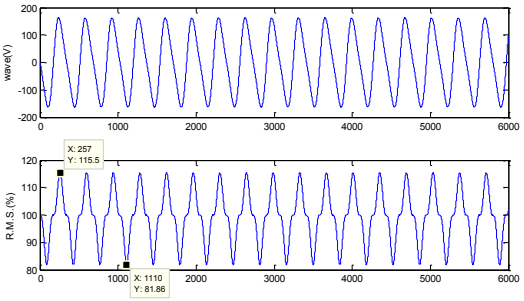

Fig. 3 contains 20% of a half cycle of the second harmonic RMS calculation

C. Power Harmonic Analysis Technology

This power harmonic analysis uses Fourier transform time-frequency domain conversion; however, the process of the discrete Fourier transform is quite complicated, by simplifying the calculation process, a faster algorithm can be obtained, this faster algorithm is called the fast Fourier transform. The Fast Fourier Transform still has the restrictions and effects the discrete Fourier transform has.

(1) Aliasing effect

According to Nyquist sampling theorem, the sampling frequency must be greater than twice the frequency of the test signal or the full details of the signal cannot be gained, resulting in a high-frequency signal becoming a low-frequency signal after sampling, resulting in signal aliasing, in Figure 4.

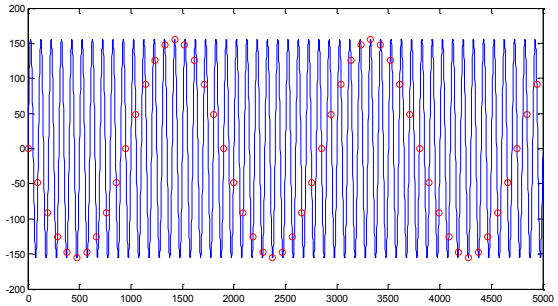

Fig. 4 Low sampling frequency aliasing caused

(2) Picket-fence effect

Since the spectrum of the discrete Fourier transform is obtained by sampling a continuous Fourier transform spectrum, just like looking at the scenery through the fence, only parts of the spectrum can be seen. So if there is a spectral component in two lines then it cannot be detected. The space between the spectrum interval is called the spectrum scale, calculated as (1) formula, where *Fs* is the sampling frequency, N represents the N-point fast Fourier transform.

$$\Delta f = \frac{F_s}{N} \tag{1}$$

(3) Leakage effect

If the input data is not exactly an integer multiple of the signal period, the signal may appear a discontinuous cut during its cycle extension. This would prevent the energy from concentrating on a certain scale and causing it to disperse to adjacent scales, which would result in lower energy and energy leakage. Eventually, this leads to a serious error spectrum, a phenomenon known as leakage effects.

IV. System Design Planning And Simulation

The calculation of power quality is highly related to signal frequency and sampling frequency. The system discussed in this paper bases on Taiwan's power frequency, which is 60Hz. According to the standard specification of IEC 61000-4-7 [9], Fast Fourier Transform calculation requires at least 0.2 seconds of continuous signal to obtain a spectrum of the spectral energy scale 5Hz, and uses it to analyze the harmonics and inter-harmonics size contained in the electrical signal. Considering the fundamental frequency of 60Hz, the calculation of 0.2 seconds of continuous signal is equivalent to calculating 12 cycles of a signal, as the time window size of the fast Fourier transform needs to be the power of 4 (the fast Fourier transform of this system is set as a radix -4 architecture), the system sampling frequency must be specially designed to meet the above two requirements.

In actual applications, the fundamental frequency is not fixed as 60Hz, there will be slight frequency change. Generally, Phase Locked Loop (PLL) will be adopted for signal frequency tracking, and real-time modification of the sampling frequency to achieve the prescribed requirements. However, this will make it impossible to know exactly the sampling frequency, and must be used in a special way. After comparing both approaches, the system in this paper uses a fixed sampling frequency design.

As a result of the fixed sampling frequency, the design of the sampling frequency is particularly important. In addition to the fast Fourier transform, the calculation of the time window size of a half-period moving window RMS is also related to the sampling frequency, one needs to know the half-cycle signal as N-point, and then can proceed to the design for N-point moving window RMS calculation module.

Since the restrictions of using fast Fourier transform to calculate is much stricter than moving window RMS calculation, in order to reduce the errors caused by a fixed sampling frequency, the restrictions and requirements of fast Fourier transform are taken into consideration for designing the sampling frequency. Sampling frequency (*Fs*) is calculated as (2) below, where the known fundamental frequency is 60Hz, 12 cycles of continuous signals are calculated, and a 4096-point fast Fourier transform module is used.

$$Fs = \frac{F \times N}{Cycle} = \frac{60 \times 4096}{12} = 20480Hz \tag{2}$$

In order to increase the possibility of the system's further development and consider the fact that future algorithms could use higher sampling frequency for the analysis of power quality events. The sampling frequency is designed to six times as originally expected, and then through the sampling point 6 the original sampling frequency can be obtained. With such a design, future algorithms can use a sampling frequency six times higher than originally anticipated to analyze the power quality. Six times the sampling frequency of 20480Hz is 122880Hz, meaning that each sampling interval is 8138ns. The system clock is set as 100MHz, where the interval between each clk is 10ns, so the system can be designed to 8140ns, which is the nearest interval to 8138ns. After countdown computing, the actual sampling frequency obtained is 122850Hz. Since the sampling frequency is set six times previously expected, the next sampling should be divided by 6, so the actual input sampling frequency of computing systems would be 20475Hz.

The constraints of system clock would affect the sampling frequency setting, the actual input computing system with a sampling frequency of 20475Hz is slightly different from the ideal sampling frequency 20480Hz. So fast Fourier transform will produce a leakage, causing errors in the spectrum. In order to understand the impact of this sampling frequency, the system uses the Matlab calculation simulation prior to its design. However, the fundamental frequency is not fixed to 60Hz, so other than simulating the input signal frequency as 60Hz, simulations of 59.5Hz as well as 60.5Hz are conducted. Fast Fourier transform calculation simulation results are shown in Figure 5, where the total harmonic distortion spectrum error rate is used as the measurable indicators. The simulation results of the maximum and minimum percentage statistics in Table 1.

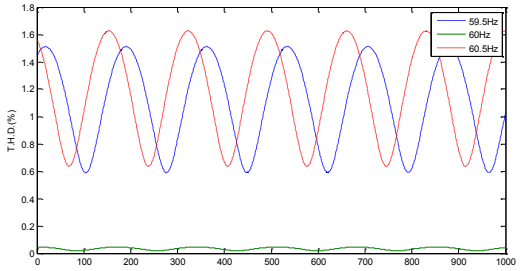

Fig. 5 Simulation results of fast Fourier transform

TABLE I
STATISTICAL SIMULATION RESULTS FAST FOURIER TRANSFORM

Freq.	59.5Hz	60Hz	60.5Hz
T.H.D.	0.5894 - 1.5115%	0.0179 - 0.0458%	0.6362 - 1.6264%

The actual sampling frequency is 20475Hz, compared with 170.625 points half-cycle, so the design of 171 points RMS calculation module to calculate a half cycle Windows Mobile rms. Since the 171 points and the actual half-cycle 170.625 points is slightly different, the RMS calculation results will produce errors. As the fundamental frequency is not fixed to 60Hz, therefore the system modeled the fast Fourier transform simulations. In addition to the 60Hz input signal frequency, simulations of 59.5Hz and 60.5Hz are also conducted. Half-cycle RMS calculation simulation results are shown in Figure 6, the simulation result of maximum and minimum statistics is shown in Table 2.

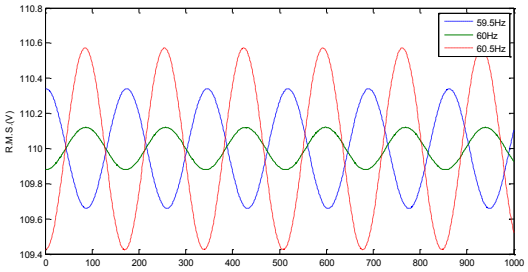

Fig. 6 RMS simulated calculation results

TABLE II
RMS CALCULATION RESULTS OF STATISTICAL SIMULATION

Freq.	59.5Hz	60Hz	60.5Hz
R.M.S.	109.6589 - 110.3401V	109.8794 - 110.1205V	109.4245 - 110.5725V

V. SYSTEM ARCHITECTURE

The system is divided into the front-end Power Quality Analyzer (PQA), and the back-end Nios II processor data display and transmission parts. The system architecture is shown in Figure 7. This two parts, through PQA interface, act as the communication medium. The front section contains the ADC controller, the sampler, fast Fourier transform module, RMS calculation modules, power quality event recognizer and the original waveform records controllers in the hardware blocks. The rear part is the Nios II processor control panel.

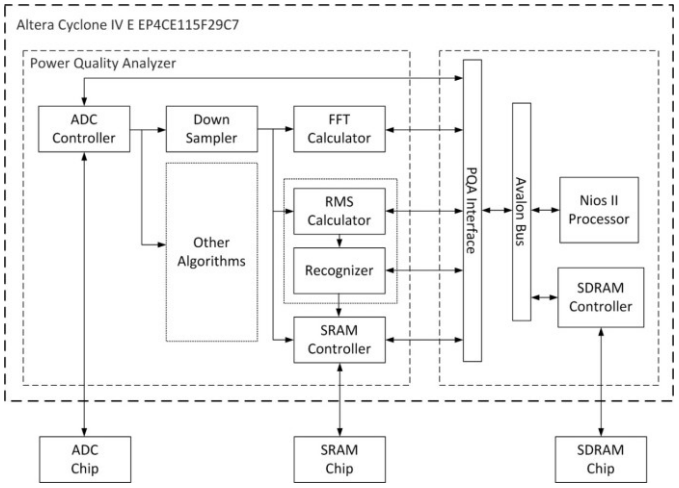

Fig. 7 System structure

A. Memory Allocation

Hardware calculation modules adopted FPGA internal memory for data access. Altera Cyclone IV E EP4CE115F29C7 builds with 3,981,312 bits RAM block. Because the hardware computing is rapid, mobile Windows RMS and fast Fourier transform computing both use a calculation module to complete an eight-channel operation, effectively reducing the use of hardware resources. This system uses a 16-bit precision A / D converters, so the size of each data 16 bits.

Fast Fourier transform module uses 4096-point FFT Module, due to the fact that the 4096 fast Fourier transform takes a long calculation time, to ensure that an 8-channel data is not overwritten by the new data before the complete, it is necessary to provide adequate buffer memory in the design. This module contains a buffer memory with each channel storing 4200 documents. The memory size used is 537,600 bits. A 4096-point FFT Module for conversion process needs to store the real and the imaginary parts, it takes a memory size of 131,072 bits. The results suggest that the real and imaginary parts are both 16 bits, it only stored half of the spectrum value 2048 documents and switched between two sets of memory storage, the memory size used is 1,048,576 bits. RMS calculation module uses 171-point RMS Module, each channel needs to store 171 documents. It uses a memory size of 21,888 bits. The calculating result is 64 bits and it switched between two sets of memory storage, the memory size used is 1,024 bits. Original waveform record controller uses Static Random Access Memory (SRAM) for its waveform data storage. Since the system uses a single-port SRAM structure, and in order to reach the goal that both the SRAM read / write actions can take place simultaneously, in places of reading and writing, a buffer memory for data adjustment is added. Both of the two buffer memories are set to 32 documents. On the writing part, 16 bits of the memory are used to record data, another 3 bits are used to store channel data. The total memory used is 608 bits, whereas the reading part, only 16 bits of the memory are used to record

data, using a memory size of 512 bits. All the various hardware modules' memory usage described above is displayed in detail in Table 3.

TABLE III
DETAILS OF THE MEMORY USAGE

模組名稱	細節列表	使用大小
快速傅立葉轉換模組	資料儲存	4200x16x8 = 537,600 bits
	FFT Module	4096x2x16 = 131,072 bits
	結果儲存	4200x16x8x2 = 1,048,576 bits
有效值計算模組	資料儲存	171x16x8 = 21,888 bits
	結果儲存	64x8x2 = 1,024 bits
原始波形紀錄控制器	Read Buffer	32x(16+3) = 608 bits
	Write Buffer	32x16 = 512 bits
總共使用		1,741,280 bits

B. Hardware Design

(1) PQA interface

PQA interface serves as a bridge for the Nios II processor and the hardware modules. It's constructed on the Avalon Bus, and therefore needs to meet the design specifications of Avalon bus [10]. Looking from a microprocessor's point of view, the PQA interface functions like a control register. Nios II processor can set or read data through the reading or writing the PQA interface data register. The control register has different designs for reading and writing. It is shown in Table 4 and Table 5.

Setting registers (write) include Reset, ADC Set, RMS, FFT and DATA and so on. Control addresses fall respectively on 0x00 - 0x20. Address 0x00 is the reset registers, which can be set to a 0 bit if resetting all hardware modules would be required; addresses 0x08 is the ADC Set register, and it can control the operational status of the ADC controller when set to 0 - 1 bits. Address 0x10 is an RMS register and can be set to a position 0 bit to determine whether the valid data read is higher or lower than 32 bits 32 bits. On the 1 bit position it is designed to determine whether if it should switch storage memory. Addresses 0x18 is a FFT register and can read the address of spectral values (1 - 2047) when set to a position 0 - 10 bits. At an 11 bit position it is set to determine if it should switch the storage memory. Address 0x20 is DATA register. When positioned at 0 bit, it can be set to determine if it will store the data onto the original waveform record registers. At the 1 bit position, the data read would be either the original waveform or the abnormal event flag. At 2 – 4 bits it is set to read the channel number of the original waveform.

Data registers (read) including RMS, FFT and DATA registers, etc., Control address is 0x10 - 0x20 respectively. Addresses 0x10 - 0x17 are RMS registers. By writing the H / L flags in the register to determine if the output data should be higher or lower than 32 bits. Addresses 0x18 - 0x1F is a FFT register. The position 0 - 15 bits are the imaginary parts of the result of FFT calculation. Position 16-31 bits are the real parts of the FFT calculation. Address 0 x20 is the DATA register, and through the rec flag in the writing register to determine if the output data is the original waveform or unusual event flags.

TABLE IV
AVALON WRITE REGISTER

Write													
		Bits											
Base	Name	11	10	9	8	7	6	5	4	3	2	1	0
0x00	Reset	-	-	-	-	-	-	-	-	-	-	-	reset
0x08	ADC Set	-	-	-	-	-	-	-	-	-	-	Set	
0x10	RMS	-	-	-	-	-	-	-	-	-	-	enable	H/L
0x18	FFT	enable	address										
0x20	DATA	-	-	-	-	-	-	-	channel			rec	enable

TABLE V
AVALON READ REGISTER

Read										
			Bits							
Base	Name	Control	31-28	27-24	23-20	19-16	15-12	11-8	7-4	3-0
0x10 – 0x17	RMS (CH0~CH7)	H/L = 0	RMS Low 32bit							
		H/L = 1	RMS High 32bit							
0x18 – 0x1F	FFT (CH0~CH7)	-	FFTresults (Actual)				FFT results (Virtual)			
0x20	DATA	rec = 0	-	-	-	-	Original wave information			
		rec = 1	-	-	-	-	-	-	-	abnormal

(2)ADC controller

A / D converters use the ADS8568 [11] introduced by Texas Instruments. It has the fastest sampling rate of 500ksps, 8-channel simultaneous sampling and handling bipolar voltage. Function setting mode is divided into hardware and software modes, the data transmission is divided into parallel and serial transmissions. In this paper, the hardware model, serial transmission method is adopted for sampling.

The ADC controller hardware structure is shown in Figure 8. By adjusting the SAMPLETIME parameters, the actual sampling time is calculated as SAMPLETIME x 10ns. According to Section IV, this paper sets the SAMPLETIME

set to 814. The control method is Finite State Machine (FSM) for function switching. The transition is shown in Figure 9. Controlled by the iCTRLsel, the four states for switching are IDLE, RESET, SET and SAMPLE. When the state is IDLE, it does not perform any actions; when the RESET state is activated, it begins to reset, defaulting the ADS8568 internal registers; When the status is SET, it will set the ADS8568 internal registers according to the CONFIG setting; when the state is SAMPLE, it will proceed to a 8-channel sampling following the time set on the SAMPLETIME. oEnable refers to whether if it should begin the output data sampling; oChannel represents the channel number; oData is the output of the sampled data. When oEnable is set at 1, it starts to export output data. A sampling is completed when all 8-channel data are exported.

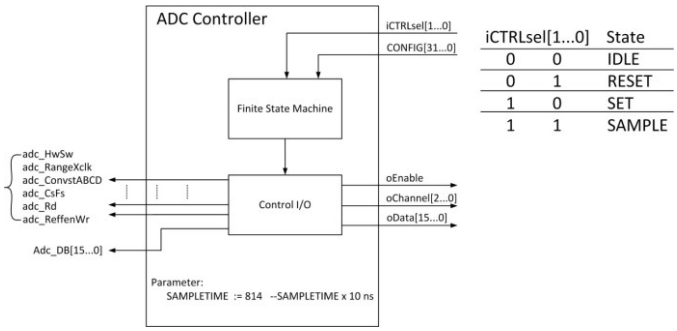

Fig. 8 ADC controller hardware structure

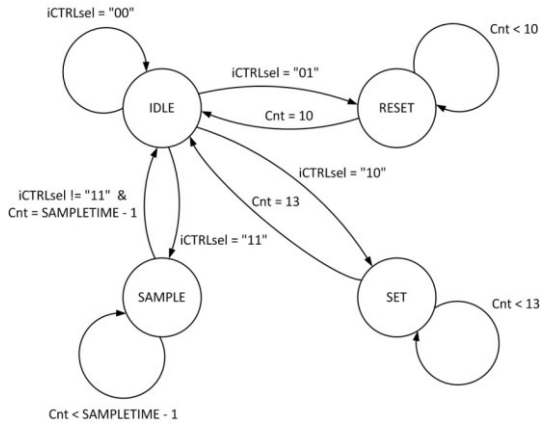

Fig. 9 ADC controller state transition diagram

(3) The sampler

In order to increase the possibility of the system's development and to consider that in the future, a sampling frequency six times higher than originally expected can be used to analyze power quality events, the sampling frequency is set to six times the originally anticipated. The data need to be processed by the sampler before being imported into the input operational modules. The input of the sampler is connected to the output of the ADC controller, and the output of the sampler is connected to fast Fourier transform module, the RMS calculation module, and the original waveform record controller. The hardware structure is shown in Figure 10. It is possible to set the DOWNPOINT parameter to adjust the sampler's ratio. According to section IV, the DOWNPOINT is set to 6. When I enable is 1, it represents the data input, and it determines if I channel is "111". If that is the case, then it is counted once. It means the A / D converter has completed a sampling. When it counts to DOWNPOINT-1, then the module internal control mechanisms will set the next input data to be directly from the module's output.

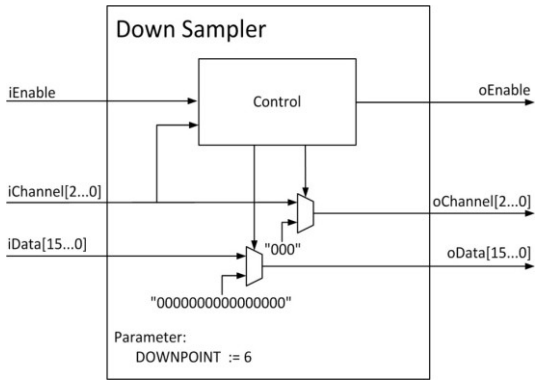

Fig. 10 next sampler hardware structure

(4) Fast Fourier Transform module

The overall design concept of Fast Fourier transform modules is based on the use of an FFT Module and by switching channels to carry out an 8-channel fast Fourier transform. As the spectral data, they are switched through two sets of memory storages. Since conducting a 4096 -point fast Fourier transform would take 286.8us. 8 channels would require a total of 2294.4us. However, a document of data is imported every 48.84us, which is way faster than the time required for an 8-channel computing. For this reason, in order to avoid the information from being overwritten before the calculations are complete, it takes an additional buffer memory of at least 47 documents per channel.

The structure of Fast Fourier transform module hardware is shown in Figure 11. There are three main parameters for setting. FFTPOINT parameter sets FFT Module time window size; MEMPOINT parameter adjusts the buffer memory size; FFTHALF parameter is used to set to save half or full spectrum values. According to Section IV, the FFTPOINT is set to 4096 and conduct a 4096 point fast Fourier transform; MEMPOINT is set to 4200, the memory space is 4,200 documents the per-channel, deducting 4,096-point fast Fourier transform calculations, there is an additional buffer space of 104 documents; FFTHALF is set to 1, because of the symmetrical nature of the spectrum, only half of the spectral values need to be stored. This module works by using finite state machine to control. The state transition is shown in Figure 12. The initial state is IDLE, when the input data has accumulated to 4096 documents, it switches to START; when the state is START, it begins to store the previously saved data into the 4096-point FFT Module for fast Fourier transform, and the state is switched into TRANSFORM;

When the state is TRANSFORM, as soon as fast Fourier transform is finished, it switches to RESET; When at RESET, it performs the initialization of 4096-point FFT Module, and determines whether it completes an 8-channel calculation. If it is not complete then it switches to START and continues to transform in the next channel. If it is complete, then it switches to IDEL. As the module's data reading, it can be done by switching to two memory blocks by rFFTen. oFFTch and oFFTaddr set its own reading channel number and frequency spectrum address. The oFFTdata is 32 bits. The anterior 16 bits are the real parts of the spectrum and the posterior 16 bits are the imaginary parts.

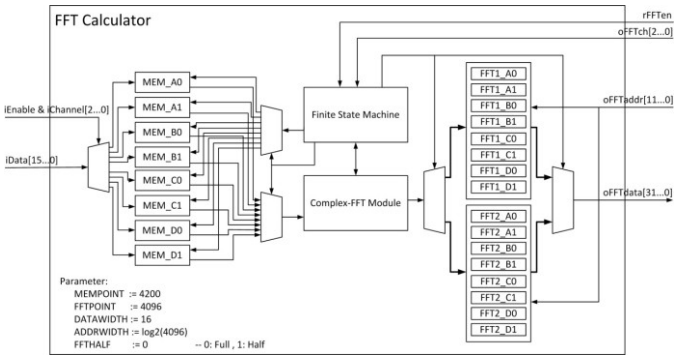

Fig. 11 Fast Fourier transform module structures

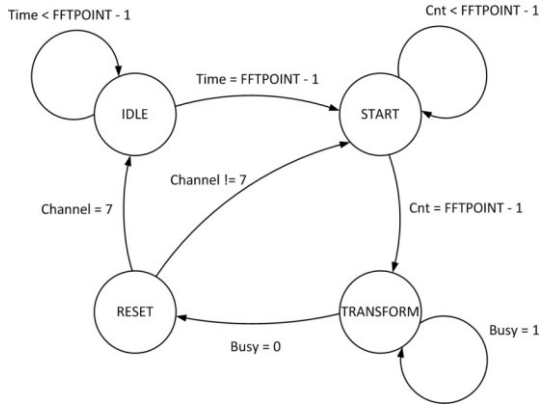

Fig. 12 Fast Fourier Transform module state transition diagram

(5) RMS calculation module

RMS calculation module only calculates the squared parts. The overall structure is the same with fast Fourier transform module. Because a 171 point square accumulation only takes 1.71us, the total of 8-channel only requires 13.68us, which is way faster than a 48.84us would take. Thus, the extra buffer memory would be redundant.

The structure of the RMS calculation module hardware is shown in Figure 13. There are two main parameters for setting, RMSPOINT parameter sets the time window size of RMS Module. MEMPOINT parameter sets the buffer memory size. According to Section IV, the RMSPOINT is set to 171, to conduct the 171 points for the mobile Windows RMS calculation, MEMPOINT is set to 171. The size of the memory coincides with the size of window, so no additional buffer space is required. oRMSen, oRMSch, and oRMSdata are connected to the input of the power quality event recognize for the detection of abnormal voltage changes. Data reading part is similar to that of fast Fourier transform module, but there are no addresses to choose from, and the rRMSdata are 64 bits.

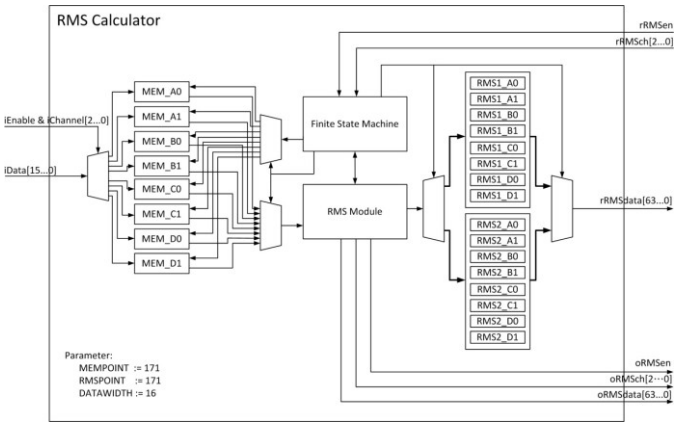

Fig. 13 RMS calculation module structure

(6) Power quality event recognizer

A power quality event recognizer contains 4 detection modules. The input end of it connects with the output end of the RMS to detect any abnormal voltage changes. Because the RMS calculation module calculates only the accumulated, squared values, if it is to find the discriminant of abnormal events, then the threshold value would have to be corrected. That is, the originally judged threshold of 110% is modified to 121%, and the sag threshold drops to 81% from 90%, and the interruption threshold is changed from 10% to 1%.

The hardware structure of the power quality event recognizer is shown in Figure 14, REFNUM_H and REFNUM_L parameters must be set to 1% of the nominal accumulated squared value, and can thus be used as the judgment of the interrupt event threshold. The parameters are then multiplied by 121 and 81 as event judgment threshold for dips & swells. Abnormal event flag oRECen is 4 bits. When the detection module detects abnormal voltage fluctuations, the detection module flag is set to 1. If REC_Module0 and REC_Module1 detect abnormal events simultaneously, then oRECen will be "0011." As to the reading part, the oRECch selects the channel number, when oRECdata's output is the squared accumulated value of the maximum (swell event occurs) or the minimum (dip or interrupt event occurs), oRECtime then exports an abnormal event duration.

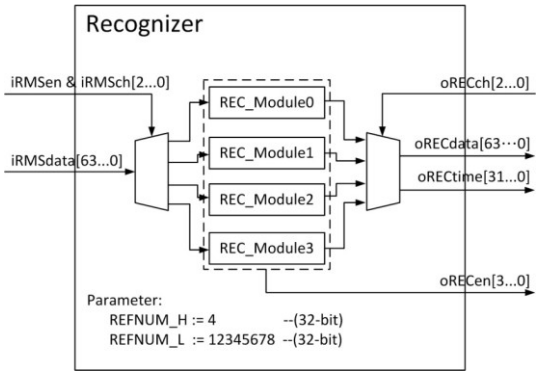

Fig. 14 power quality event recognizer hardware structure

(7) The original waveform record controller

When an abnormal event happens, a 10 cycles before and after the event of sampling data have to be stored for subsequent analysis. Because the huge amount of data, the external SRAM memory is then used as a storage medium. Due to the use of single-port SRAM, only one read / write can be carried out simultaneously. Read / write at a different timing cannot be conducted. In practical cases, what might happen is that during the read / write process, another read / write process may be required. The latter read / write operation will be ignored. In order to simplify the design and consider that the writing operation of the system only functions at the input end, and the reading operation functions on the output end, the buffer memories for data adjustment are added on the two ends respectively. Details of the operation are shown in Figure 15, when the SRAM of the information has already stored 20 cycles and ReadStart is 1, the read memory starts to fill. When the data in the read memory is only half left, the filling starts again until all the data is read. When the reading memory becomes full or when the read is complete, it will start checking whether there are data in the write memory. If there is any data in it, then it will be written into the SRAM.

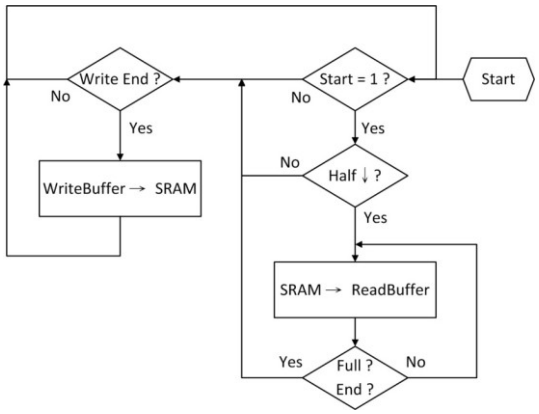

Fig. 15 SRAM read / write operations can be allocated flowchart

Original waveform record controller contains 8 addresses controller that are used to record the access address of an eight-channel data. Each address controller has a dedicated iRECen, and is connected with oRECen of the power quality events Identifier. When iRECen is 1 then the address controller begins to record. The address controller divides the SRAM memory into 16 sets by storing the address (Two sets of memory blocks per channel each). Each memory block size contains 20 cycles of data items. The records are shown in Figure 16. The data input has been saved to MEM_0, when iRECen is 1, it represents an occurrence of an abnormal event. It continues to store data until after 10 cycles, it switches to MEM_1 to continue to store data. This way it retains an anomaly occurs 10 cycles of data around MEM_0.

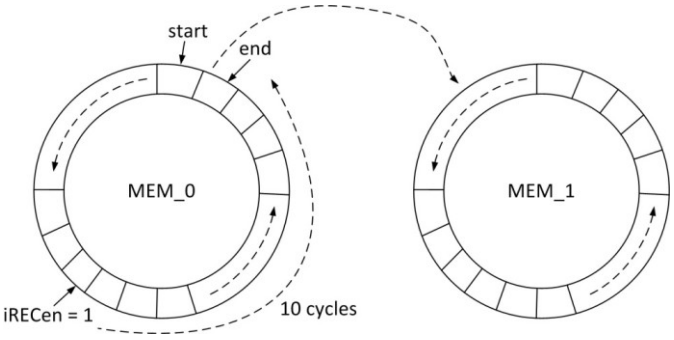

Fig. 16 SRAM storage methods

The hardware structure of the original waveform record controller is shown in Figure 17. There are three main parameters for setting. SRAMPOINT parameter needs to set 20 cycles of data items; RMEMPOINT and WMEMPOINT parameters are used to set the read / write buffer memory size. According to Section IV, a cycle has about 341data items, 20 cycles would have 6820 data items, so SRAMPOINT is set to 6820; RMEMPOINT and WMEMPOINT are set to 32. In terms of the reading part, ReadCh must be set first to read channels. Then set ReadStart as 1 and begin to put the SRAM data into read memory, and then observe whether there is data in read memory through ReadNum. Finally through ReadEn and ReadData for data reading action.

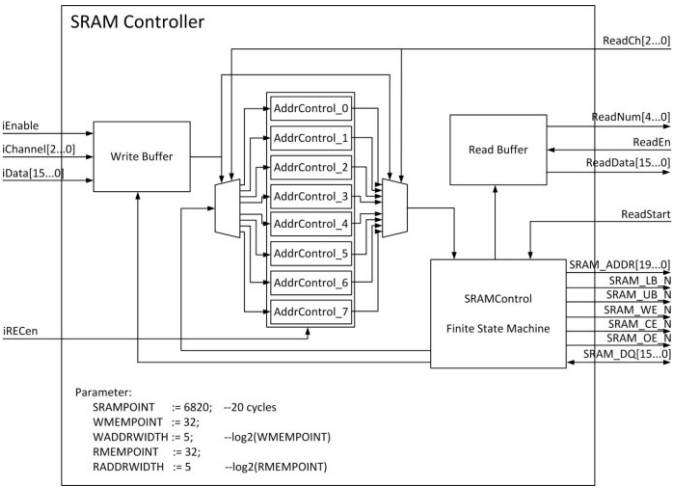

Fig. 17 original waveform recording controller hardware architecture

C. System Action Process

The procedures of the system developed in this paper is shown in Figure 18. When the system is running start, Nios II processor begins the initialization of each hardware module. Following that is the setting of ADC controller and then begins the samplings. The data proceed to retrieve data through the sampler. The results are then imported to Fast Fourier Transform and RMS calculation modules to carry out 12-cycle-time window fast Fourier transform and half cycle mobile window rms calculations. The output end of the RMS calculation module voltage channel connects with the power quality event recognizer for the detection of abnormal movements. When an abnormal event occurs, the power quality event reader will notify the original waveform record controller to start to record. The record will have a total of 20 cycles, before and after the incident.

Through the PQA interface, Nios II controller can read spectral values, RMS and when an abnormal event happens such as the original waveform data for further analysis.

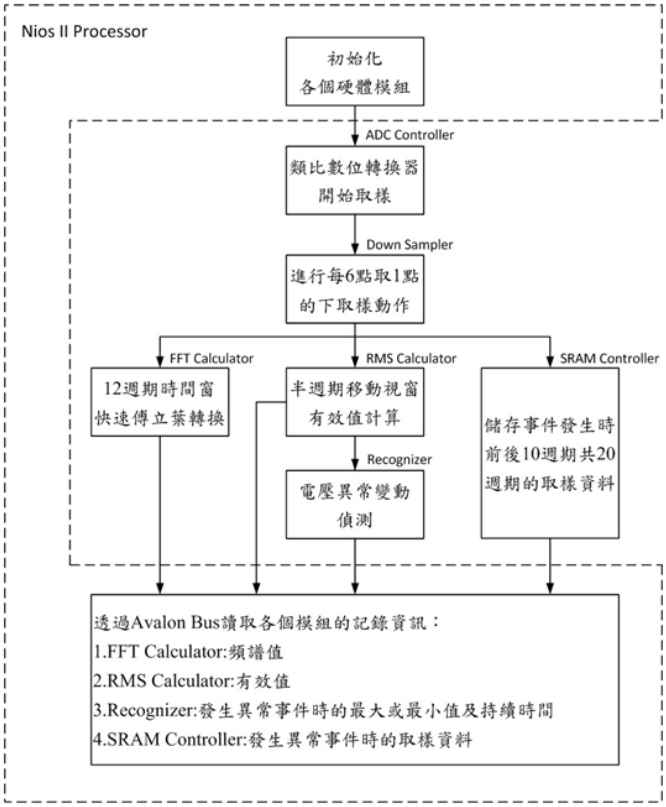

Fig. 18 System Flow

VI. Experimental Results and Validation

This chapter tests and validates the system. To begin with, this part will first explain the equipment used in the experimental part of the test, including system calibration, frequency variation tests, changes in voltage transient detection and harmonic analysis.

A. Experimental Platform and Test Equipment

(1) Altera DE2-115 platform

Altera DE2-115 platform adopts the Cyclone EP4CE115 FPGA, which is a chip that has the maximum capacity from the Cyclone IV E series, it provides 114,480 logic units and a RAM up to 3.9 Mbits and 266 multipliers. In addition, it also inherits the diverse application interfaces of DE2 series, which meet the demand for various types of research and development applications, the product appearance is shown in Figure 19.

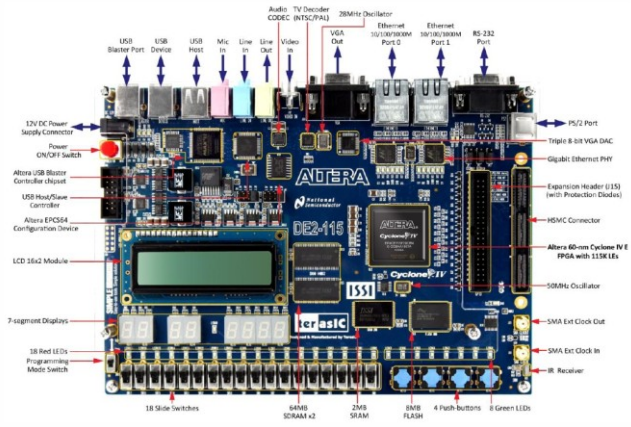

Fig. 19 Altera DE2-115 Development Platform [12]

(2) FLUKE 6100B Electrical Power Standard

Fluke 6100B Electrical Power Quality Calibrator provides pure sine wave, harmonic component signals, etc. for users to carry out calibration and verification system accuracy. In this paper, it is used for systematic correction and harmonic accuracy testing. The appearance of the instrument is shown in Figure 20.

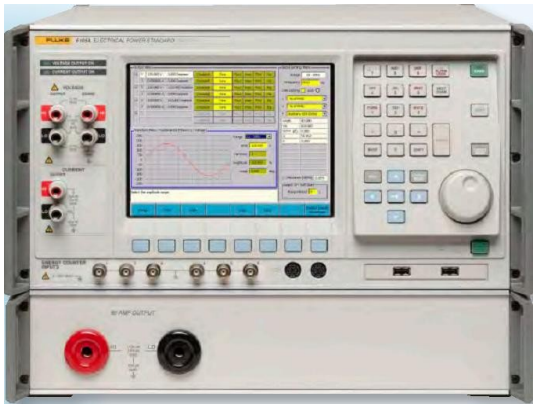

Fig. 20 FLUKE 6100B Power Standard

(3) EAB Modular Programmable AC Power Supply

EAB Modular Programmable AC Power Supply focuses on the standard application of IEC 61000-4-11, it allows setting of the start angle, voltage dips, short interruptions and a

variety of voltage changes, and it has 50 memory groups with each memory group able to set 9 test steps. Memory group and the steps can set loops individually, among groups of memory is also able to link tests to simulate various load power characteristics. In this paper, it performs voltage dips, swells and interruptions test. The appearance of the instrument is shown in Figure 21.

Fig. 21 EAB Modular Programmable AC Power Supply

B. Measurement Correction

While the analog signals transfer into digital signals, in addition to voltage transformers and current transformers conversion errors, the thermal noise, analog circuit noise and other problems can cause signal distorted measurements. Therefore, after converting a digital signal, it needs for a measurement error correction. In this study, the 110V 60Hz pure sine wave generated by FLUKE 6100B Electrical Power Standard for corrective action.

After the system imported the pure sine wave, it will obtain thousands of values and calculates the mean. It then compares with 110V to find the correction coefficient K. After this as long as the rms calculated by the system is multiplied by the correction coefficient, then the exact values can be obtained.

$$RMS_{new} = K \times RMS_{old} \tag{3}$$

C. Frequency changes test

Because the system uses a fixed sampling frequency, it has a much lower tolerance for frequency changes. Before the system was designed, the Matlab simulation has been conducted. A detailed simulation results can be found in section IV.

And the actual test of the system in this experiment uses 59.5, 60 and 60.5Hz pure sine wave produced by FLUKE 6100B Electrical Power Standard for testing. Figure 22 is the measured results of a Fast Fourier transform, the spectrum of which uses the total harmonic distortion error rate as the measurement indicator. The statistical results are shown in Table 6. Figure 23 is an rms value of the measured results, the statistical results are shown in Table 7.

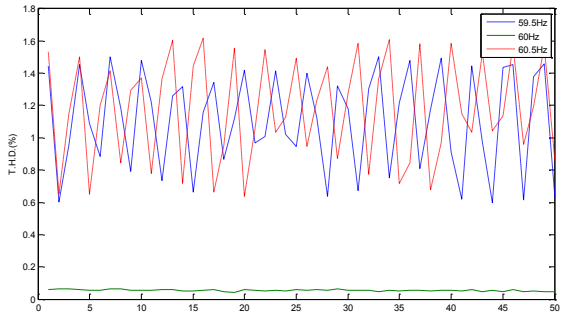

Fig. 22 Fast Fourier Transform measured results

TABLE VI
STATISTICS MEASURED RESULTS FAST FOURIER TRANSFORM

Freq.	59.5Hz	60Hz	60.5Hz
T.H.D.	0.5789 - 1.5083%	0.0386 - 0.0938%	0.6256 - 1.6305%

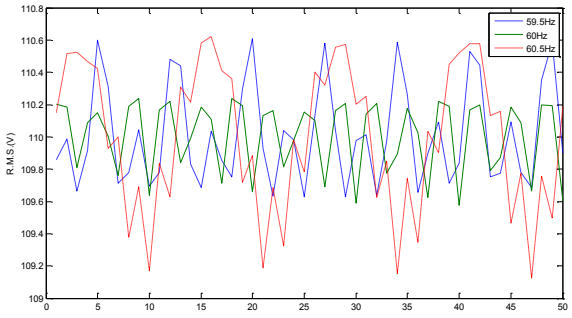

Fig. 23 RMS calculation measured results

TABLE VII
RMS CALCULATION MEASURED RESULTS STATISTICS

Freq.	59.5Hz	60Hz	60.5Hz
R.M.S.	109.5597 - 110.6754V	109.5029 - 110.2762V	109.0749 - 110.6444V

D. Detection of changes in voltage transient

This experiment adopts an EAB modular programmable AC power supply to design voltage dips, swells and interrupt events to simulate transient voltage changes. When the system detects an abnormal event, it will record 10 cycles of waveform before and 10 cycles of waveform after an abnormal event occurs, and then records the highest (voltage swells case) or the lowest (voltage sag or interruption) voltage value and an abnormal duration of the event, the data in this experiment validate these three comparisons. First, it reads a total of 20 cycles of waveform data and then through the Matlab, calculates the rms of a half cycle mobile window. It then identifies and calculates the maximum or minimum voltage value and its duration. Lastly, it compares with the record of the system to verify the accuracy of the system.

(1) Test voltage swells

EAB Modular Programmable AC Power Supply output is set to rise from 110V to 132V and it continues for two cycles. Figure 24 is the setting of the AC power supply. It sets 132V and continues for 33.3ms. Figure 25 is a swells waveform captured by transient recorder. Figure 26 is the detection results of the system. The image display includes the duration, maximum voltage and a total of 20 cycles of waveform data before and after the abnormal events. Figure 27 uses Matlab to show a 20 cycle wave data and conducts a half-cycle window RMS calculation. The calculation result shows an unusual events continuation of 688 points, and a maximum voltage of 132.8V, which is consistent with the system record.

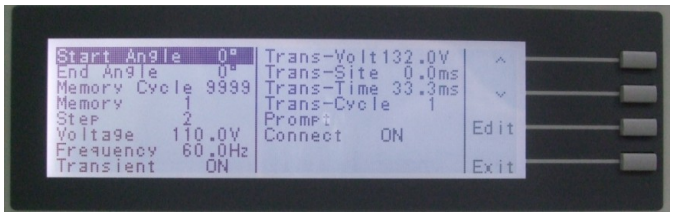

Fig. 24 the AC power supply output sets 132V continues 33.3ms

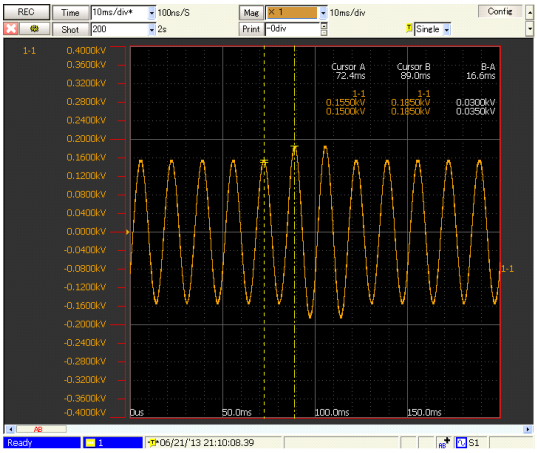

Fig. 25 Swells waveform captured by the transient recorder

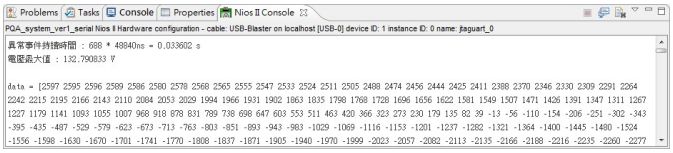

Fig. 26 system shows the voltage swells

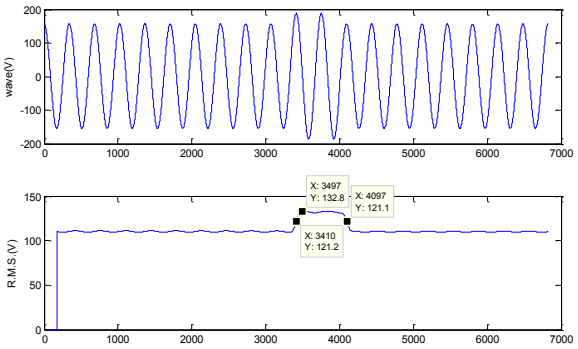

Fig. 27 Matlab verifies the voltage swells detection.

(2) Voltage dip test

EAB Modular Programmable AC Power Supply is set to dip from 110V to 88V and continued for two cycles. Figure 28 is the setting of AC power supply. It is set to 88V and continued 33.3ms. Figure 29 is a captured image of the sagged waveforms of a transient recorder. Figure 30 is the results of the detection of the system. The screen display shows abnormal events including the duration, the minimum voltage, and a total of 20 cycles of waveform data before and after abnormal events. Figure 31 shows a 20 cycle wave data as well as conducts a half-cycle mobile window RMS calculation. The calculation result shows a 676 points of continuation of unusual events. The minimum voltage value is 86.94V, which is consistent with the system record.

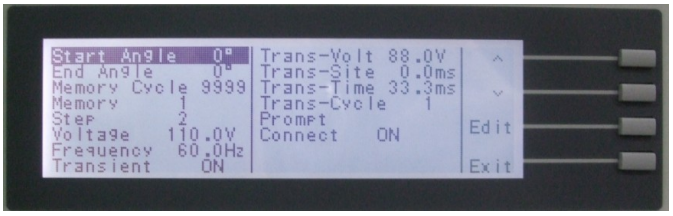

Fig. 28 AC Power Supply Set Output 88V continues for 33.3ms

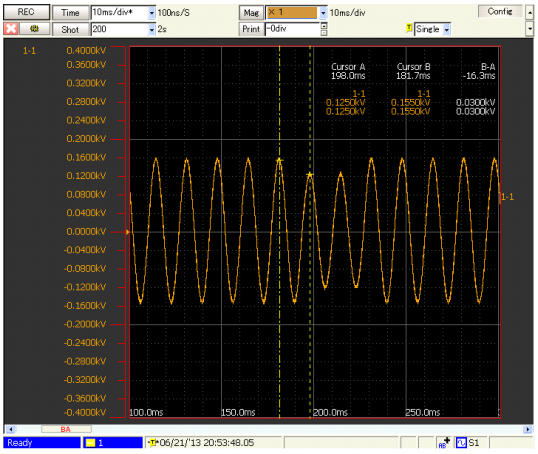

Fig. 29 dips waveform captured by transient recorder

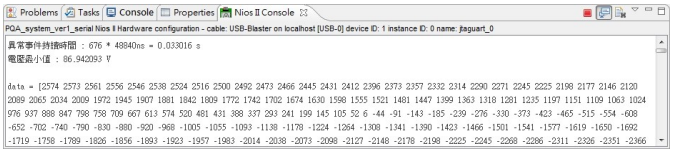

Fig. 30 System Shows the Voltage Sag Information

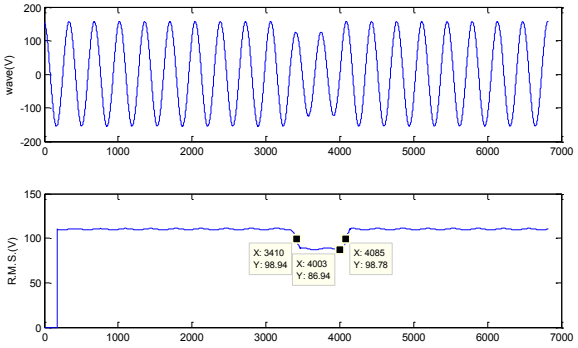

Fig. 31 in Matlab, voltage sag detection verification

(3) Voltage interruption test

Voltage-Interruption test sets EAB modular programmable AC power supply output to dip from 110V to 5.5V and continues for two cycles. Figure 32 shows an AC power supply setting. It sets 88V and continues for 33.3ms. Figure 33 is the waveforms captured by a transient recorder. Figure 34 is the detection results of the system. The screenshot shows a few things including the duration of abnormal events, the minimum voltage, and a total of 20 cycles of waveform data before and after the occurrence of abnormal events. Figure 35 shows a 20 cycle wave data as well as conducts a half-cycle mobile window RMS calculation. The calculation result shows a 741 points of continuation of unusual events. The minimum voltage value is 4.196V, which is consistent with the system record.

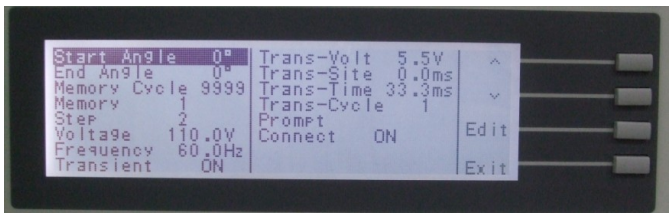

Fig. 32 AC Power Supply Set Output 5.5V continued 33.3ms

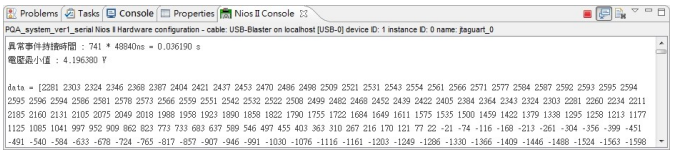

Fig. 33 Shows the Voltage Interrupt Information System

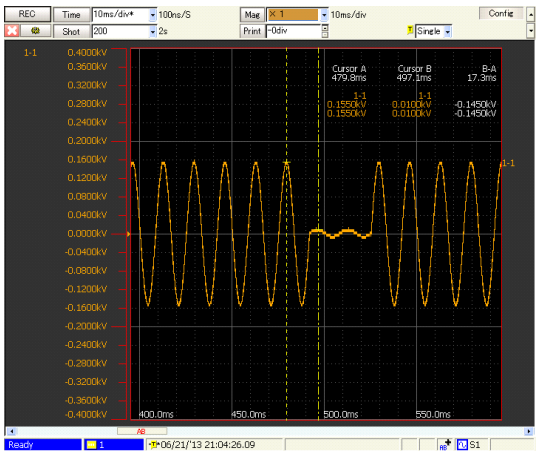

Fig. 34 Transient Recorder Captured Waveforms

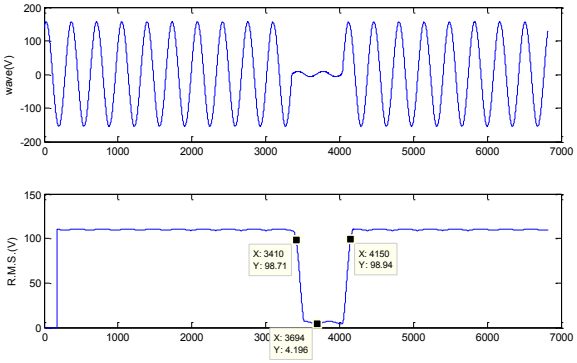

Fig. 35 Matlab for Voltage Detection Interrupt Verification

E. *Power Harmonics Measurement*

The main goal of this experiment is to test the accuracy of the system for the even and odd harmonics measurement. In the actual tests, FLUKE 6100B Electrical Power Standard contains harmonic signals. A secondary and tertiary harmonic test of 0.5%, 1.0%, 2.0%, 5.0%, 10% and 20% were conducted. Test results are expressed in percentages, as shown in (4). The THD system is the system measurement results. THD is the harmonic components set by the input signal. When the percentage is a positive sign, it means the measurement results is far greater than the actual setting of the harmonic; when it is negative , it means the measurement results is much smaller than the actual harmonics set. The second harmonic test results are shown in Figure 36, the tertiary harmonic test results are shown in Figure 37, each set of test result statistics are in Table 8.

$$Error(\%) = \frac{THD\_system - THD}{THD} \times 100\% \qquad (4)$$

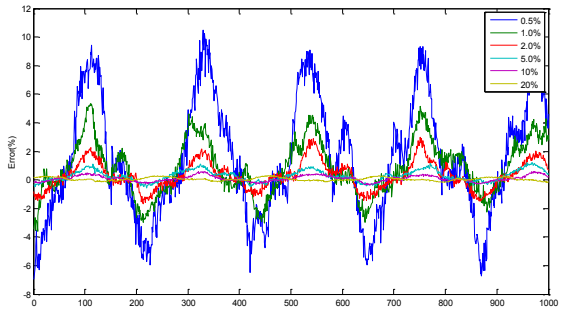

Fig. 36 Second Harmonic Error Results

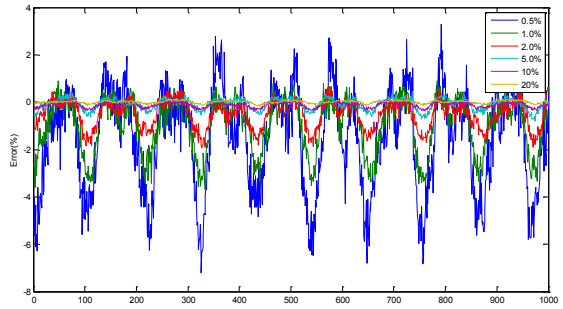

Fig. 37 Third Harmonic Error Results

TABLE VIII
GROUP HARMONIC TEST ERROR STATISTICS

T.H.D.	secondary armonic	tertiary harmonic
0.5%	-6.9572% - 10.5058%	-7.2014% - 3.2970%
1.0%	-3.6173% - 5.3375%	-3.6934% - 0.9968%
2.0%	-1.6729% - 2.9911%	-1.9208% - 0.6814%
5.0%	-0.5632% - 1.2122%	-0.7904% - 0.3843%
10%	-0.3776% - 0.5877%	-0.3558% - 0.1307%
20%	-0.1835% - 0.3113%	-0.1843% - 0.1480%

VII. CONCLUSIONS

Power Quality is the major problem power company and the users have to face currently because of poor power quality such as voltage abnormal movements, power harmonic interference, phase imbalance and so on will cause long-term electrical and electronic equipment damages, reducing its expectancy life and failures, a serious accident may even directly endanger people's lives and property.

The power quality recognition system developed in this paper focuses mainly on power quality transient voltage changes and power harmonic wave interference detection. To ensure the sampled data value for research analysis, a fixed sampling frequency is adopted. Since the sampling frequency is based on the signal of 60Hz power, the system's tolerance for power frequency changes is low, the further away the frequency is from 60Hz, then the more inaccurate it will be. According to Section VI C, the measured results show that at 59.5Hz, the maximum harmonic distortion rate is 1.5083%, the RMS is between 109.5597 and 110.6754V; when it is at 60Hz, the maximum harmonic distortion rate is 0.0938% , the RMS is between 109.5029 and 110.2762V; and when it is at 60.5Hz, the maximum harmonic distortion rate is 1.6305%, and the RMS is between 109.0749 and 110.6444V. We can conclude that the total harmonic distortion is more sensitive to changes in supply frequency, the RMS calculation is not obvious, this part of the simulation results match Section IV.

About transient changes in voltage detection, apart from detecting voltage dips, swells and interruptions, it also records the highest (voltage swells case) or lowest (voltage sag or interruption) voltage value and the duration of unusual events. In addition, a total of 20 cycles of sampling data, both with a 10 cycle before and after the abnormal event, are recorded for preservation. Detailed test results are described and validated in VI section D.

And about power harmonic wave analysis, a 4096 -point fast Fourier transform is used to calculate 12 cycles of data, the spectrum scale is 5Hz, it can analyse frequency harmonics and inter-harmonics up to 10.24kHz. In Section VI E, it conducted a measurement accuracy test of the harmonic wave analysis. The total input harmonic wave distortion signal is 1%, the second harmonic wave error is below 5.5%, and the third harmonic wave error is less than 5 %.

ACKNOWLEDGMENT

Courtesy of NSC "Transmission System Power Quality Monitoring Technology Development and Application of NSC 102-3113-P-194-002" for the funding.

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