Embedded Test Technology of Switching Power Supply Based on FPGA

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Abstract—**In this paper, an embedded test technology of switching power supply based on FPGA was introduced to solve the shortcomings exist in the traditional detection methods, such as the complex process of maual detection, long test time, maintenance and support difficult, high cost of maintenance, etc. The FPGA implementation has been achieved on the Cyclone EP2C35F672C6. The results show that it can realize the automatic detection of switching power supply, improve the fault detectionrate and isolation rate of switching power supply, shorten the test time, reduce the test difficulty, improve the life cycle of switching power supply, reduce the life cycle cost of switching power supply, and this equipment is feasible and versatile.**

***Keywords*—FPGA; Switching Power Supply; Embedded Test Technology**

I. INTRODUCTION

With the rapid development of power electronics technology and manufacturing technology, switching power supply showing the trends of integration, miniaturization and complex, which makes the traditional method of using the probe detection to detect the switching power supply more difficult[1]. This paper presents an embedded test technology of switching power supply based on FPGA, it can realize the automatic detection of switching power supply, improve the fault detectionrate and isolation rate of switching power supply, shorten the test time, reduce the test difficulty, improve the life cycle of switching power supply, reduce the life cycle cost of switching power supply, and this equipment is feasible and versatile.

II. EMBEDDED TEST DESIGN OF SWITCH POWER

The development of social and technology makes the increasingly popularity of PC, PC become more and more important in the work and life of people[2]. Given the breadth and importance of PC and the important role of power supply in PC, it's necessary to do the embedded test design for the PC power supply. This paper views P4-320A switching power supply as a sample for embedded test design.

A. Switching Power Supply Parameters

Table I shows the input parameters of P4-320A, Table II shows the output parameters of P4-320A.

TABLE I
P4-320A INPUT PARAMETERS

input	parameter
AC input	220V
I_{max}	3A
f	50Hz-60Hz

TABLE II
P4-320A OUTPUT PARAMETERS

DC output	I_{max}
+3.3V	11A
+5V	14A
+12V	8A
-5V	0.5A
-12V	0.5A

B. Principle of Switching Power Supply

P4-320A is consist of aid power supply and main power supply, the functional block diagram show as Fig. 1.

Auxiliary power auxiliary main supply, auxiliary power and the main power sharing a rectifier modules. Auxiliary power is consist of the input rectifier module, pulse transformers, switching converter, the output rectifier filter module, sampling circuit, self-excited circuit. Mains is consist of the input rectifier module, pulse transformers, switching converter, the output rectifier filter module, sawtooth generator circuit, PWM pulse generating circuit, a protection circuit, optical coupling circuit, sampling circuit.

When the switching power supply is powered on, the auxiliary power supply starts to work, generates +22 V and +5 V DC voltage, +22 V and +5 V supply the main power chip and a part circuit of the power, and the +5 V supply the motherboard power management module. In this case, the main power supply is not working. When you press the PC power button on, the motherboard sends a PS (Power Start) signal to the main power supply, then the main power supply begin to work. When the main power supply detects that the output voltage is normal, then the main power supply will send a PG (Power Good) signal to the motherboard. When the motherboard receive the PG signal, it will enter the normal boot process, if the motherboard does't receive the PG signal, then the boot failure.

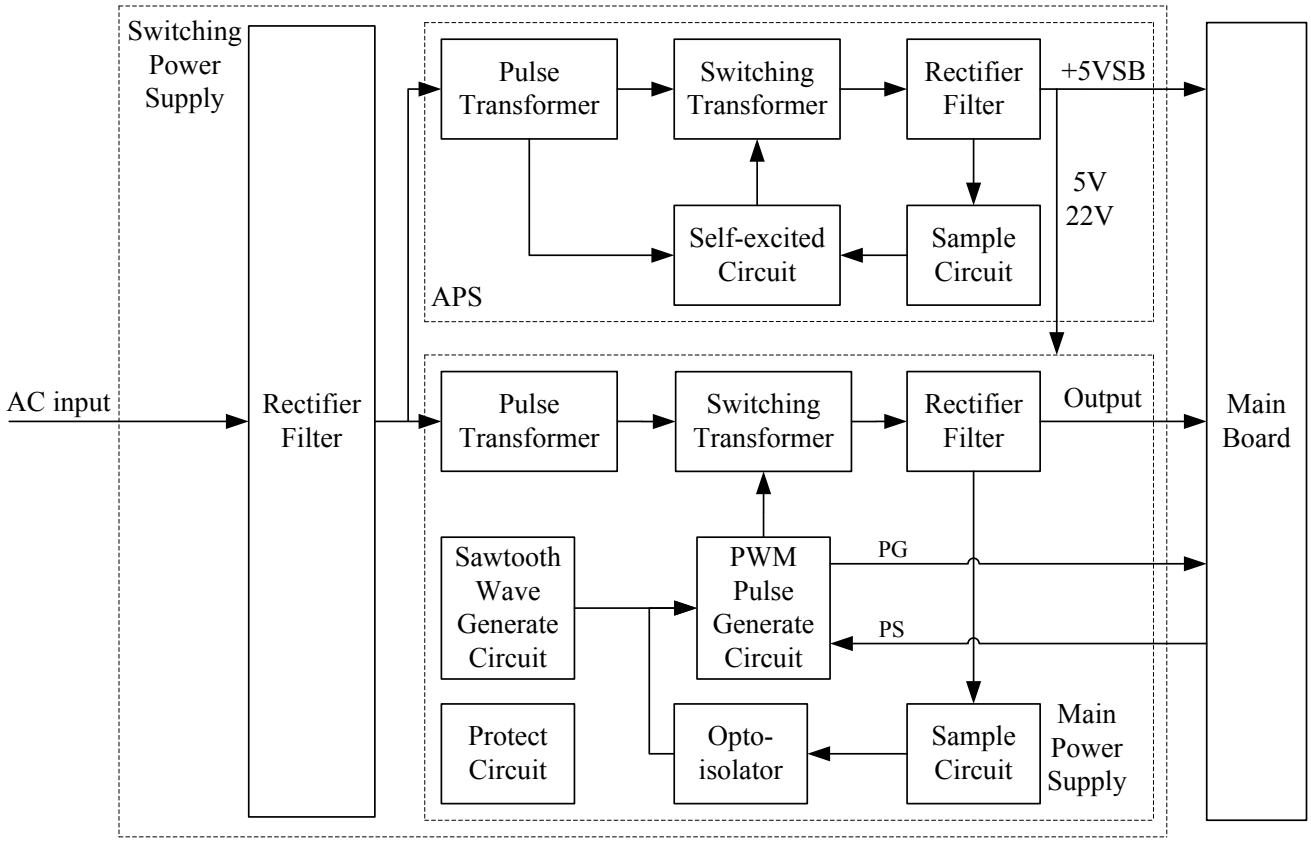

Fig. 1 P4-320A functional block diagram

C. Common Faults of Switching Power Supply

The circuit of P4-320A is complex, it contains a wide range of electronic components, so the possible of failure is also virous. Table 3 shows the probability of various common switching power failure. It can be seen from Table III that the switch tube breakdown, blowout, high voltage filter capacitor damage, rectifier bridge damage, Schottky rectifier diode breakdown short circuit, output filter capacitor damage accounted for 96%, other failures accounted for only 4%. When switching power supply has faults, mostly, it's single fault not composite fault. So, in the actual fault diagnosis, diagnosing the single fault not the composite fault is feasible and effective in the project.

TABLE III
FAULT PROBABILITY OF VARIOUS COMMON SWITCHING POWER FAULT

Fault Type	Probability
switch tube breakdown	26%
blowout	22%
high voltage filter capacitor damage	17%
rectifier bridge damage	14%
Schottky rectifier diode breakdown short circuit	10%
output filter capacitor damage	7%
others	4%

D. Test Point Design

According to the selected set of faults, conbine the principle of P4-320 and the experience of using and maintenance of P4-320, set 8 test point as shown in Table IV.

TABLE IV
TEST POINT LIST

Test Point	Position
TP1	Collector of Switch Tube in Switch Converter of Auxiliary power
TP2	+22VOutput
TP3	+5VOutput
TP4	Input After Fuse
TP5	Output of Rectifier Filter
TP6	Primary of Pulse Transformer
TP7	Main Power+12VOutput
TP8	Main Power+5V Output

III. SWITCHING POWER SUPPLY FAULT DIAGNOSIS ALGORITHM FPGA IMPLEMENTATION

Currently, in the field of fault diagnosis algorithm, emerging of a lot of new research hotspot, such as artificial neural networks, fuzzy inference identification method, wavelet transform analysis, expert system, etc., but in actual

using, the most effective fault diagnosis algorithm is the fault dictionary method[3]. Take the specific circumstances of switching power supply, this paper use fault dictionary method to diagnose the switching power supply, and use FPGA to realize it.

E. Fault Dictionary Method

Fault dictionary method, also known dictionary databases diagnosis[4]. This method works in the analysis of the specific circuit based on the combined use of equipment maintenance experience, select the fault set, set the test point, and then through the large number of real experiments, simulations and simulation analysis, the failure to obtain a collection of all the test points corresponding to the output response , the establishment of test points and fault response output correspondence between eigenvalues, and the relationship with certain tabular form in storage, called fault dictionary. When performing fault diagnosis, by finding fault dictionary can diagnose faults[5]. Fault Dictionary Method with targeted, diagnostic advantages of speed. Fault Dictionary Method difficulty lies in the process of establishing fault dictionary, fault dictionary richer, the diagnostic capacity of the stronger.

F. FPGA Implementation of Fault Dictionary Method

Fault Dictionary Method for FPGA Implementation block diagram shown in Fig. 2. There decision block diagram, sequence generation module fault and fault dictionary. Test point information generated by the decision module after the test point indicator bit indicating that the point is normal. Failure sequence generation module consists of eight test points to obtain fault indication bit sequence, and then by the failure sequence to find fault dictionary, fault diagnosis results obtained, the final output.

There is determined the module during normal operation switching power supply test point information, the module will enter the test point information with the stored information of the correct test point compared to the test point is determined whether it is normal, if normal, the output is 0, if normal output is 1. Failure sequence generation module eight test points indicate bits splicing operation to obtain fault sequences. Fault exists in the dictionary experiment, simulation analysis to obtain the fault dictionary, according to the sequence of the resulting failure to find fault dictionary, you can get fault diagnosis.

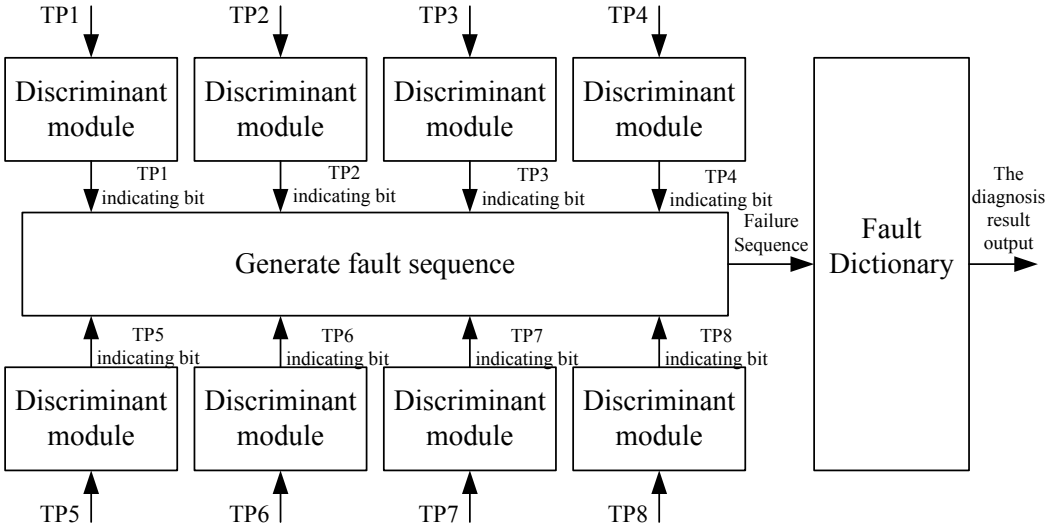

Fig. 2 Block Diagram Fault Dictionary Method FPGA Implementation

1) Decision Module

Identification module FPGA realization diagram shown in Fig. 3. Signal test points (TP) and the maximum coefficient obtained by multiplying the upper threshold (TP_UP); test point signal and lower coefficient to obtain lower threshold (TP_DOWN). Then test point signal and the upper threshold for comparison, if greater than the upper threshold, the output 0 and less than the upper threshold output 1; test point signal and the lower threshold for comparison, if greater than the lower threshold, the output 1, is less than the lower threshold output 0. Be done with the two output operation signals so that if the test points within the threshold range, the output 1, output 0 otherwise. And the power in the actual boot process, there will be an output voltage settling time, typically 1ms, obtained within this time bound test point signal is not normal, so the results of operations to be performed on the median filter, the length of time taken is 15ms, the sampling time of 1ms, set at 15 cycles, 10 or more times if the same result, then take the result as a final result of the discrimination, the otherwise discarded. RTL determination module shown in Fig. 4.

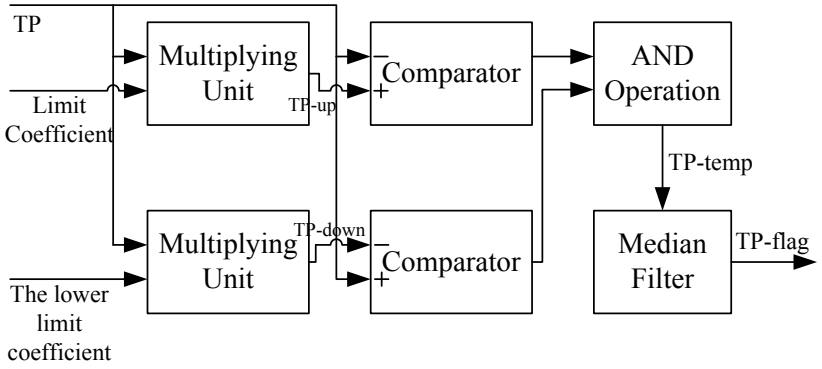

Fig. 3 Discriminant Block Diagram

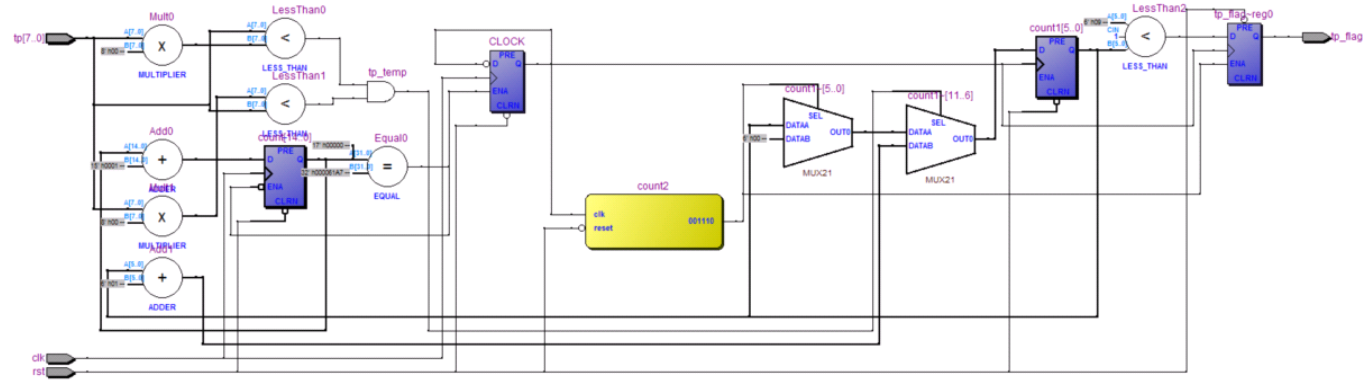

Fig. 4 RTL in Discriminant

2) Failure Sequence Generation Module

Failure sequence generating method shown in Fig. 5. The TP_flag1 to TP_flag8 as splicing operation. TP_flag1 is 0, TP_flag2 as a, TP_flag3 of two, TP_flag4 to 3, TP_flag5 to 4, TP_flag6 of 5, TP_flag7 to 6, TP_flag8 to 7, thereby generating a fault sequence.

3) Fault Dictionary Module

Dictionary to be stored due to a fault information and fault test point the relationship between the characteristic values, and thus customize a ROM, 8 bits wide each memory cell of the storage unit 256. Then the fault sequences as fault dictionary ROM address lookup, you can get fault diagnosis. RTL fault dictionary module shown in Fig. 6.

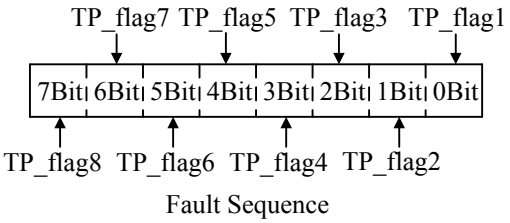

Fig. 5 Fault sequence generating method

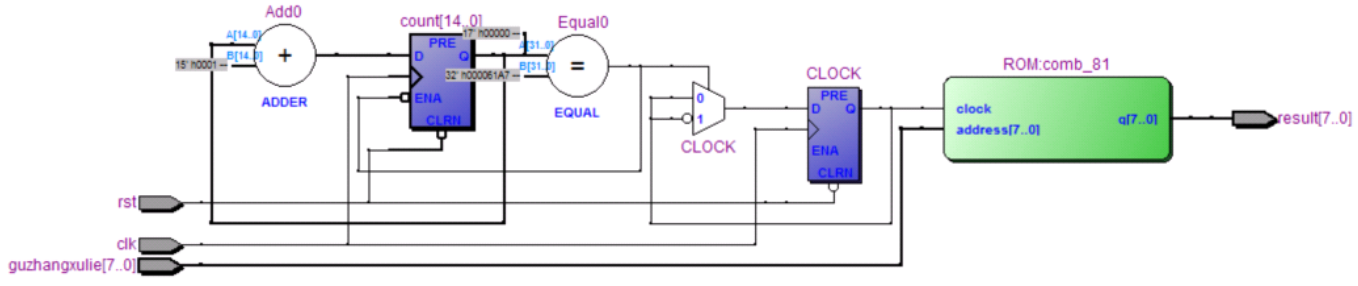

Fig. 6 RTL of Fault Dictionary Module

IV. System Implementation and Results Analysis

In order to verify this technique, hardware platform designed experiments.

A. Overall System Block Diagram and Real Object

Overall system block diagram shown on the left in Fig. 7. Switching power supply embedded test system include the power input module, input pre-module, processing module voltage, A/D converter module, FPGA module and display module. The real objcet of the switching power supply embedded test system is shown in Fig.8. Theh left in Fig.8 is the input prefix module and FPGA module, the middle is the sample power, the right is the voltage treatment module and the ADC.

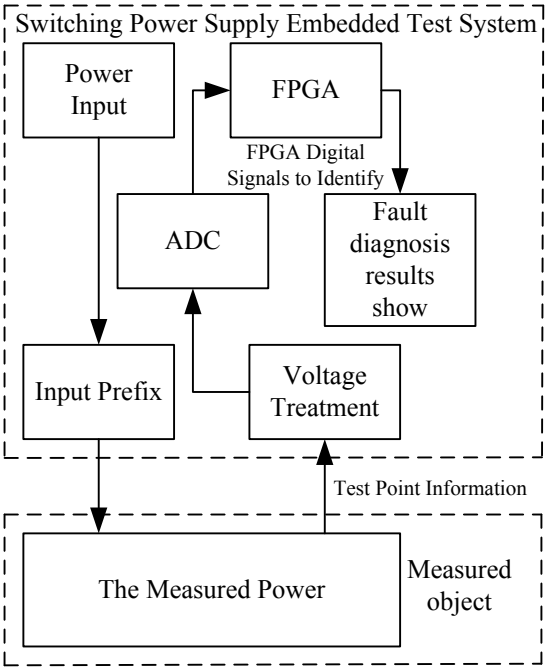

Fig. 7 Switching Power Embedded Test System Block Diagram

B. FPGA Simulation Results

For this article to be implemented FPGA fault diagnosis algorithm for modelsim simulation, the results shown in Fig. 9.

Fig. 8 Real Object of the Switching Power Embedded Test System

C. System Measured Results

In this paper the identified fault set, this paper designed switching power embedded test system is an ambiguity in the case, the fault detection rate of 100%, fault isolation rate was 55.6%; fuzzy degree 2 in the case of , 100% fault detection, fault isolation rate of 77.8%; the ambiguities in the case of 4, the fault detection rate of 100%, 100% fault isolation.

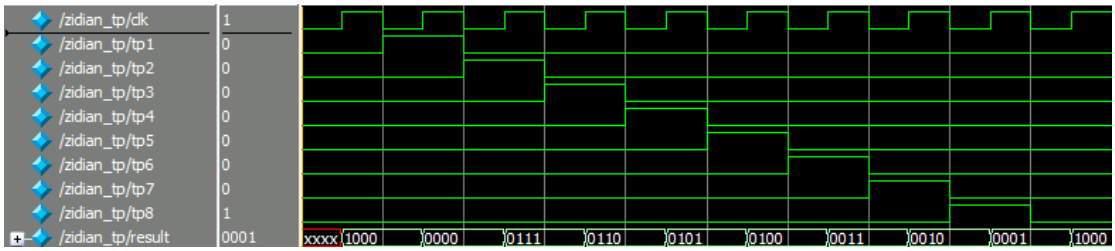

Fig. 9 FPGASimulation Results

D. System Measured Results

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V. Conclusion

Testability in the full study theory and fault diagnosis technology, based on the switching power supply design for testability, we propose a FPGA-based embedded test technology switching power supply, and accordingly build a switching power embedded test system. Finally, building

hardware test platform for the switching power embedded systems has been verified. The fault diagnosis technology in the field of switching power supply provides a new method, the new Silk Road, there is a certain value and reference.

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