The Permanent Magnet Synchronous Motor Vector Control System Based on FPGA

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Abstract— **In this paper, an FPGA chip and the external circuit is to achieve permanent magnet synchronous motor vector control system. Using Altera's Cyclone III EP3C25Q240C8N, rich programmable logic on-chip resources are utilized to realize the vector control of the system. Moreover, the right circuit of sampling and conditioning is the key point to the reliability of Closed-loop system. Finally, the experimental results show that Speed can follow the instruction and closed-loop system is reliable.**

***Keywords*— FPGA；Vector control；Closed-loop system**

I. INTRODUCTION

Permanent magnet synchronous motor(PMSM) has the advantages of simple structure, small volume, high efficiency, low moment of inertia, easy to be heat dissipation and maintaining etc. Especially, with the decline in the price of permanent magnet materials, the improvement of magnet materials performance, and the emergence of new magnetic materials, using Permanent magnet synchronous motor (PMSM) in the high precision, high reliability, small power, wide speed range of servo system has attracted many researchers. However, PMSM model is multi-variable, strong coupling and nonlinear, so making the control system is more complex and expensive than DC motors. German F. Blashke proposed a vector control principle in 1970s, by using it，making the PMSM control can mimic the DC motor control which can gain efficient performance, so then using PMSM is increasingly popular in the areas of high performance AC drive. In recent years，because of abundant logic and layout resources, FPGA (Field Programmable Gate Array) as the master chip has become a research focus in servo motor control [1-2], Firstly, the parallel processing method greatly improve computing speed. Secondly, it can be planned into a dedicated control chip so that can accords with needs of a variety of motor control. This paper discusses the FPGA-based permanent magnet synchronous motor vector control system, the chip is Altera's Cyclone Ⅲ EP3C25Q240C8N.

II. CONTROL PRINCIPLE

By using the vector rotation transformation and rotor flux orientation, the motor stator current can decompose into excitation and Torque. The excitation is consistent with the direction of the magnetic field, and Torque is advanced by 90^o. Permanent magnet synchronous motor Stator winding pass into a three-phase sinusoidal current and each phase sinusoidal current difference 120^o. The rotor poles is compose with permanent magnet, sinusoidal magnetic field is produced in the air gap. The sinusoidal magnetic field is fixed on the rotor position so that the synchronous rotation shaft in the vector control coincides with the rotation of the rotor shaft. The synchronous rotation shaft is d-q axis. PMSM's torque angle δ change with the load, control and maintain $\delta = 90^0$，then it can achieve decoupling control，this is the rotor magnetic field oriented vector control.

A. Mathematical model of permanent magnet synchronous motors

Vector control principle was originally aimed of the induction motor, its theory can be directly extended to synchronous motor. Permanent magnet synchronous motor's rotor use high energy product permanent magnets for magnetic pole, without slip rings and brushes. Rotor pole produce sinusoidal magnetic in the air gap, induce sinusoidal electromotive force in the stator. Making the following assumptions of Permanent magnet motor model：

1) Ignoring eddy current and hysteresis loss.
2) Ignoring core saturation
3) stator electric potential varies by sine law, the stator current only produce sinusoidal magnetic potential in the air gap.
4) No damper winding on the rotor, the permanent magnets have no damping effect.

For the optimized design model of permanent magnet synchronous motor, through Park transformation, its d-q coordinate system mathematical model is as follow and The derivation process can reference in [3-4].

$$\frac{di_{ds}}{dt} = \omega_e \frac{L_{qs}}{L_{ds}} i_{qs} - \frac{r_s}{L_{ds}} i_{ds} + \frac{V_{ds}}{L_{ds}} \quad (1)$$

$$\frac{di_{qs}}{dt} = -\omega_e \frac{L_{ds}}{L_{qs}} i_{ds} - \frac{r_s}{L_{qs}} i_{qs} + \frac{1}{L_{qs}} V_{qs} - \frac{1}{L_{qs}} \omega_e \lambda_f \quad (2)$$

$$T_e - T_l = J_m \frac{d\omega_r}{dt} + B_m \omega_r \quad (3)$$

$$T_e = \frac{3}{4} P \lambda_f i_{qs} \qquad (4)$$

$$k_t = \frac{3}{4} P \lambda_f \qquad (5)$$

i_{ds}、i_{qs}: The d、q axis stator current of Permanent magnet synchronous motor on d-q coordinate system.
L_{ds}、L_{qs}: The d、q axis stator inductance of Permanent magnet synchronous motor on d-q coordinate system.
V_{ds}、V_{qs}:The d、q axis stator voltage of Permanent magnet synchronous motor on d-q coordinate system.
r_s: motor stator winding resistance.
T_l: load torque.
T_e: motor torque.
k_t: motor torque constant.
P:Number of poles.
B_m: Lagged coefficients .
J_m: moment of inertia.
ω_e : Electrical speed.
ω_r : rotor mechanical speed .
λ_f :Permanent magnet synchronous motor magnetic flux on d-q coordinates.

By the above formula (1-5) can be obtained schematic diagram 1，from it we know that there are still some physical coupling. But by using the way of decoupling, physical coupling model can be completely decoupling then you can control q-axis in order to control motor torque. When the current controller (such as P or PI Controller) is added in the d-axis or q-axis, it becomes the control block diagram, shows in Figure 2. When the d-axis current is given as 0, the output current i_{ds} can be controlled to 0, indeed, it can get completely decoupled state. Therefore, when control $i_{ds} = 0$, The model of PMSM (Figure 2)can be simplified, the new model of d-q axis show in Figure 3.

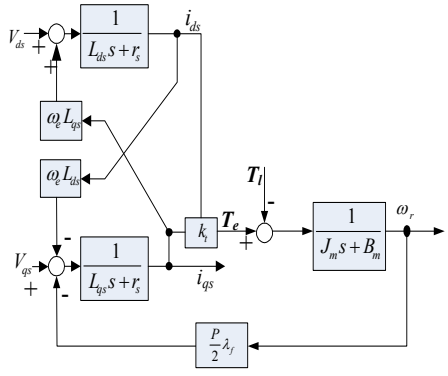

Figure 1.d-q coordinates motor model

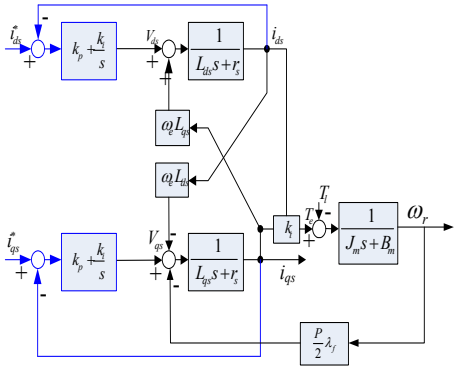

Figure 2. Join controller in the motor model

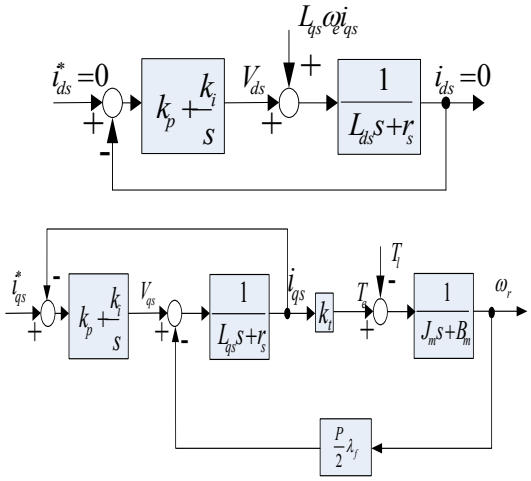

Figure 3. Completely decoupled motor d-q coordinates model

B. Coordinate Transformation

In the new model of d-q axis, we know that it can control motor torque by controlling the q-axis current. But the actual motor system is three-phase, first of all, we must change three-phase coordinate system into two axes perpendicular coordinate.

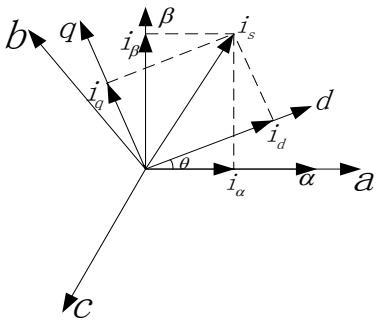

Figure 4. Stator current space vector

In Figure 4, a-b-c is three-phase stationary coordinate system, α-β is the two-phase stationary coordinate system, d-q is the two-phase rotating coordinate system. Current i_s is defined as:

$$i_s = i_a + e^{\frac{2\pi}{3}i} i_b + e^{-\frac{2\pi}{3}i} i_c \qquad (6)$$

Three-phase stationary coordinate system turn into the

two-phase stationary coordinate system is Clark transformation. the condition is power constant when Coordinate transform before and after ,then we have:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} \quad (7)$$

The relationship between two-phase stationary coordinate system and two-phase rotating coordinate system (Park transformation) is as follow:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (8)$$

The relationship between two-phase rotating coordinate system and two-phase stationary coordinate system (Park^{-1} transformation) is as follow:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \quad (9)$$

III. Overall System Profiler

Overall control of vector control system shows in Figure 5, the digital hardware system including SVPWM module, PI controller module, angle and speed detection module, vector control module and A/D control module. SVPWM module can reference in[5-6], PI controller can reference in[7], the A/D control module design is relatively simple, just refer to the chip's relationship between timing control and data transmit, the specific circuit is not given here.

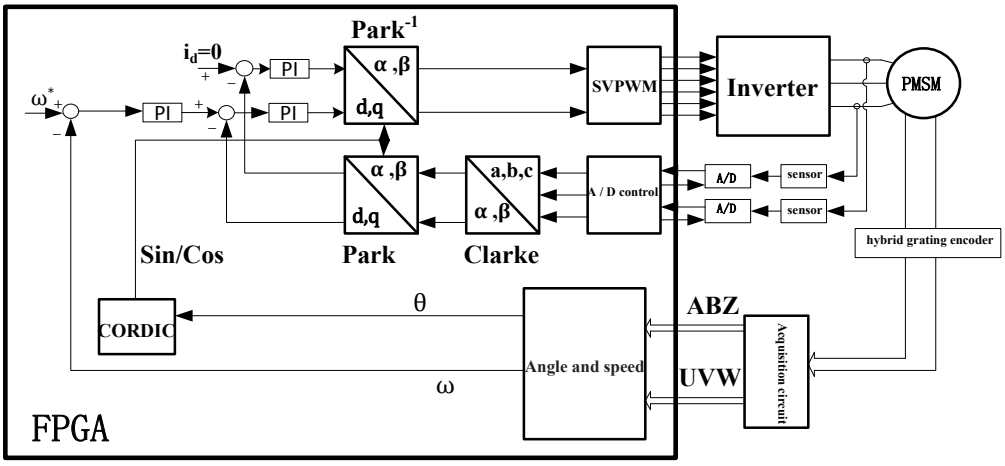

Figure 5. Vector control system

A. peripheral hardware circuit design

The current sampling circuit is shown in figure 6. Sampling the permanent magnet synchronous motor stator current, is divided into 5 areas, the first component is a voltage follower, because this circuit has a large input impedance, and small output impedance, improving the circuit with a load capacity. The second part of the signal amplifying unit, since the current, which goes through the hall sensor and becomes very small in order to obtain the appropriate data, is enlarged. The third part of the signal uplifting unit, as a result of the analog input of the ADC chip is a single-phase, the input voltage range is between 0~5V. The fourth part of the design is to change it into a second-order active low-pass filter unit. This can better filter out signals above the cut off frequency of the signal. The final link of the analog-digital conversion unit (not shown) is to convert from analog into digital quantity, then into the FPGA.

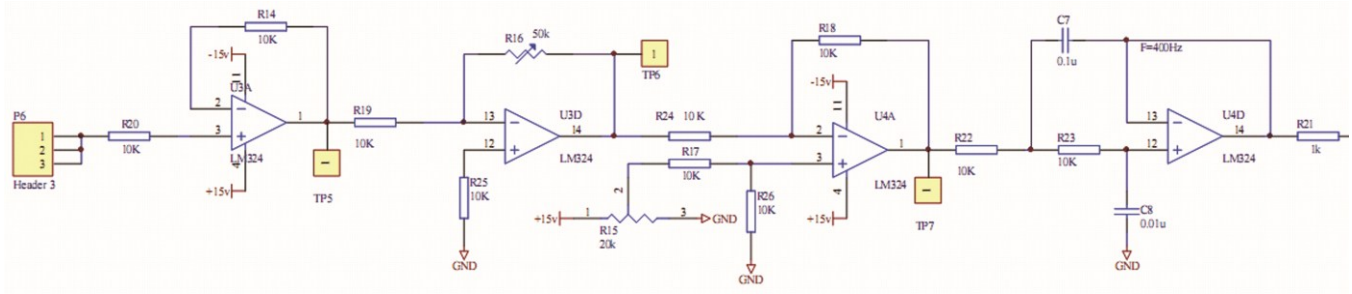

Figure 6.Current sampling circuit

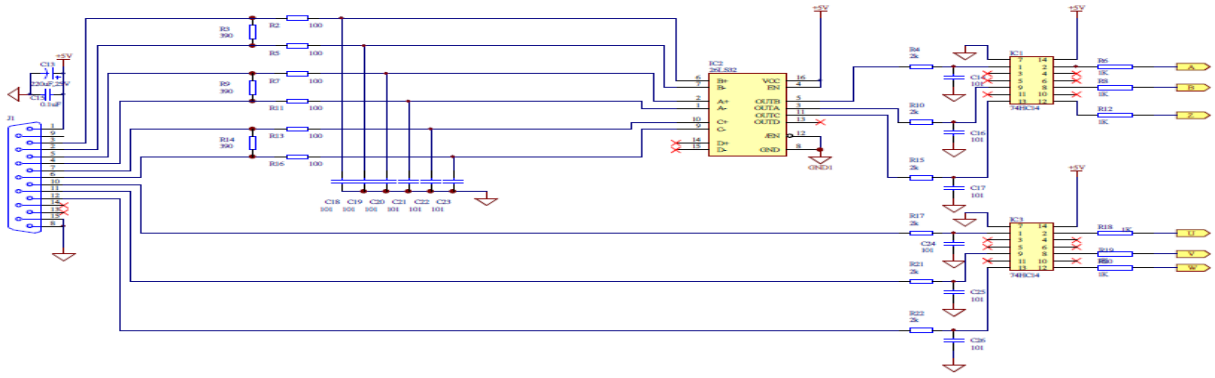

Figure 7. Regulating circuit of hybrid grating encoder

The regulating circuit of hybrid grating encoder: the signals from hybrid grating encoder contains the speed, direction and position of the motor , so correct signal regulating circuit is the key point to keep the normal operation of motor, the circuit diagram shows in Figure 7. Signals A, B, Z from hybrid grating encoder is the differential, Firstly, through a simple RC filter circuit. Secondly, use the chip 26LS32 to regulate then use the chip 74HC14 to reverse, the last, should reduce the voltage by the chip LVC4245A and then give into the FPGA. Signals U, V, W from hybrid grating encoder is used for initial the position of permanent magnet synchronous motor, This type signal processing way only need to reverse and then reduce the voltage, then into the FPGA.

Note: the output voltage of regulating circuit is about 5V, but the input voltage of the FPGA chip I/O port is about 3V, so you must reduce the voltage. The part of chip LVC4245A is not shown in the Figure 7.

B. design on the FPGA chip

Vector transformation module includes Clark, Park and Park^{-1} transformation. The hardware multipliers are used to achieve Clark transformation on the FPGA chip. And for the Park and Park^{-1} transformation, it involves Sine and cosine. There are about three ways (Taylor series method, look-up table method, Coordinate Rotation Digital Computer) to achieve Sine and cosine on the FPGA chip**.** Taking the two aspects of occupied logic resources and control precision into consideration, we choose Coordinate Rotation Digital Computer (CORDIC). its iterative formula is:

$$\begin{pmatrix} x_{i+1} \\ y_{i+1} \end{pmatrix} = \cos\theta_i \begin{pmatrix} 1 & -S2^{-i} \\ S_i 2^{-i} & 1 \end{pmatrix} \begin{pmatrix} x_i \\ y_i \end{pmatrix} \quad (10)$$

$$z_{i+1} = z_i - \theta_i = z_i - S_i \times \arctan 2^{-i} \quad (11)$$

z_i is the difference between the actual angle and each rotation angle . The direction signal S_i , which is defined as: when $z_i \geq 0, S_i = 1$; otherwise. $S_i = -1$. X_{in}, Y_{in} input is reference vector coordinates, θ_{in} is the rotation angle, range is (0^o, 360^o), but the CORIDC is only valid within the range (-99.88^o, 99.88^o). Therefore, before the beginning of the iteration, it needs to do some preprocessing, the process is:

$$\theta = \begin{cases} \theta_{in} - \frac{7\pi}{4} & \frac{3\pi}{2} \leq \theta_{in} \leq 2\pi \\ \theta_{in} - \frac{5\pi}{4} & \pi \leq \theta_{in} \leq \frac{3\pi}{2} \\ \theta_{in} - \frac{3\pi}{4} & \frac{\pi}{2} \leq \theta_{in} \leq \pi \\ \theta_{in} - \frac{\pi}{4} & 0 \leq \theta_{in} \leq \frac{\pi}{2} \end{cases} \quad (12)$$

First of all the input X_{in}, Y_{in} Multiply a constant gain

$$K = \prod_n \cos\theta = \prod_n \sqrt{\frac{1}{1+2^{(-2i)}}} = 0.607252935,$$

Thus it avoids multiplication in the iterative process.

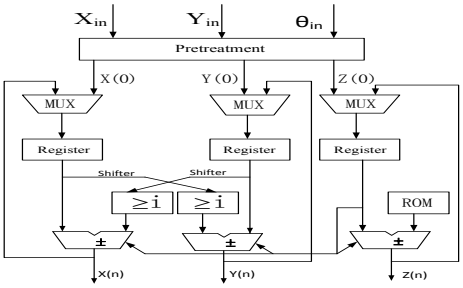

Figure 8.CORIDC hardware circuit design

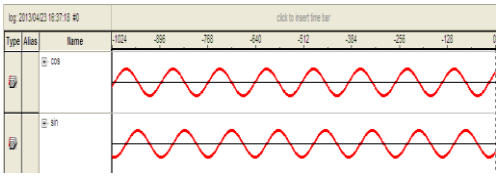

Figure 9.Sine and cosine waveform

Figure 8 shows the CORIDC hardware circuit, digitized basic rotation angle (binary an 22-bit) is stored in the ROM table, and Addition, subtraction and shift operations achieve

by the adder, subtractor and shifter on the FPGA chip. Finally, taking on-chip resources, algorithm accuracy and processing speed into consideration, we choose the number of iterations is 20 views, accuracy better than 0.003%. We use a signed Q19 of 21-bit format to represent angle (range from 0^o to360^o) in the experiment, iterative calculation work out the value of Sine and cosine at the same time, the waveform of logic analyzer shows in Figure 9.

The detection module of position: the signals of the speed, position are computed by the U, V, W, A, B, Z signals which come from hybrid grating encoder. Signals U, V, W are used for initial positioning of the motor, Z pulse signal (each lap generates one) eliminate the accumulated error. In order to increase the accuracy of motor's position, in general, the Frequency of A, B pulse signals is multiplied by four. Figure 10 shows the design diagram of the speed, position, because the counting circuit is very sensitive to interference signals, if there have no noise filter, the counter will make a mistake [8]. Therefore, we should do first digital filter processing.

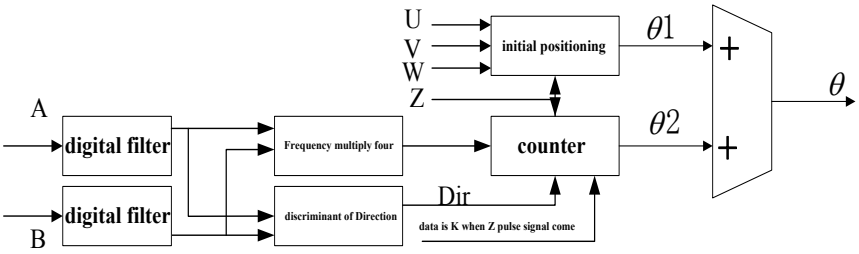

Figure 10 . design diagram of the position

IV. EXPERIMENT

The parameters of Permanent magnet synchronous motor: rated power is 750W, rated current is 3.58A, rated speed is 3000rpm, grating digital of the encoder is 2500PPR. The Switching frequency of IGBT(Insulated Gate Bipolar Transistor) is 10KHZ,and the frequency of current sampling is same, speed sampling frequency is 2KHZ, the deadtime is about 3μs. Experimental platform shows in Figure 11.

The modules are designed by using VHDL(Very-High-Speed Integrate Circuit Hardware Description Language) in this paper, The report of the closed-loop system is shown in Figure 12. From the report ,we can see the share of logic resources is relatively little (5269 LEs, proportion is 21%), the figure 13 shows speed is from 0 to 300r/min, view from the waveform, response time is less than 50ms, the maximum overshoot and steady-state error are small. Experimental result shows that the system has good dynamic performance.

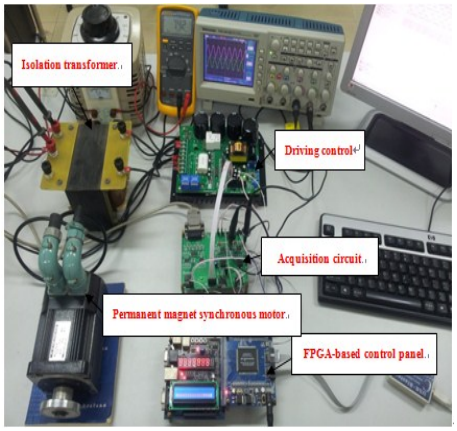

Figure 11. Experimental Platform

Flow Status	Successful - Sat Jul 13 15:39:00 2013
Quartus II Version	9.0 Build 235 06/17/2009 SP 2 SJ Web Edition
Revision Name	close_loop1
Top-level Entity Name	close_loop1
Family	Cyclone III
Device	EP3C25Q240C8
Timing Models	Final
Met timing requirements	N/A
Total logic elements	5,269 / 24,624 (21 %)
Total combinational functions	4,376 / 24,624 (18 %)
Dedicated logic registers	2,394 / 24,624 (10 %)
Total registers	2394
Total pins	74 / 149 (50 %)
Total virtual pins	0
Total memory bits	196,608 / 608,256 (32 %)
Embedded Multiplier 9-bit elements	28 / 132 (21 %)
Total PLLs	2 / 4 (50 %)

Figure 12. Compilation Report

Figure 13. Velocity waveform

V. CONCLUSIONS

This project, we get start several months ago, gain hardware design experience on the FPGA chip. we use hardware description language to achieve the system ,and if we use Nios CPU in the design, the system will be more flexible. Finally, Thanks our teachers and friends for their academic guidance and material support and also Thanks the competition organizers give us this opportunity to show our works.

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