

Design of PET Bottle Cap Defect Online Detection System Based on FPGA

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Abstract— This paper designed an online detection system based on FPGA, which was used to detect if there is defect in the internal and external ring of the PET bottle cap and stains in the steal of the bottle cap. Based on the hardware platform whose core processor is EP4CE115F29, taking advantage of the parallelism and pipeline of the FPGA ,this system detect the internal ring, external ring and the steal of the bottle cap , then make a judgement. The MegaWizard module named Median Filter was used to smooth the image and threshold value segmentation was used to extract the part in which we are interested, and then judge whether there is stain in it. We used the projection of the gray level to get the center of the bottle cap, and then comparing with the center gravity to judge if the bottle cap is qualified. What is more, the edge detection arithmetic named Scharr was used to calculate the circular degree of internal ring, then judge if there is a defect. By experimenting repetitively, the arithmetic is useful that the system can detect the PET bottle cap efficiently. The number of the bottle cap detected the bottle is more than 50000, and the detection precision is 3.

Keywords— PET bottle cap; defect detection; smooth process; threshold value segmentation; edge detection

I. INTRODUCTION

Polyethylene terephthalate (PET) is environmental protective plastic, which is used to produce drink bottle widely. At present, the number of the plastic bottle cap and bottle in our country is on top in the world. However, there must be some disqualify product in the manufacturing produce, and it is necessary to make a quality detection. But we have even no a thorough technology now, and it is mainly depend on the labour. Because the number of bottle cap produced in one second is more than 10, and the speed of labour detection can not match the speed of product line. Obviously, an online detection system that is cheap and efficient is badly in need.

Field-Programmable Gate Array (FPGA) has characteristics of parallelism handling mechanism, powerful operation capacity and flexible repeat programming. With that, FPGA has obviously advantages in digital signal processing, especially in image processing.

This paper has designed an online PET bottle cap detection system based on FPGA. The system that make full

use of operation parallel and pipeline of FPGA detect the bottle cap parallel and operation pipeline, which greatly shortens the period of detection.

II. HARDWARE PLATFORM OVERALL DESIGNING SCHEME

Hardware platform overall design mainly includes the lighting system, drive control system, image capturing and processing system based on FPGA and display system with VGA. The hardware framework of the system is shown in Fig. 1. Being powerful, the laser sensor once inducted bottle cap, the drive control module will stop the conveyor. At the same time, FPGA will capture an image to be processed later. The digital image information will be successively grey processed, threshold segmentation, smoothed and detected edge. The judgement message coming from the image processing will be send to drive control module to make the rejecting device work, rejecting the disqualification. The key link of the system is capturing and processing image efficiently.

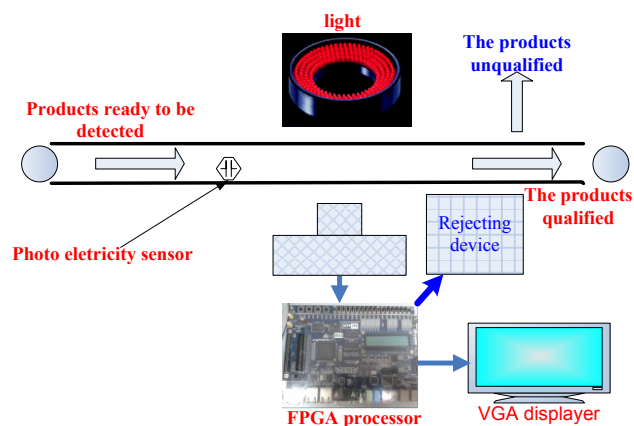


Fig. 1 The hardware framework of the system

Considering the volume of the bottle cap, we choose the ultrasonic sensor as the external triggering of the image capturing. The voltage values of ultrasonic sensor ranges

from 0.2V to 4.5V. We get better edge of trigger signal with the compared circuit formed by operational amplifier LM358. After comparing, the trigger signal of the ultrasonic sensor is switched with level 74LVC4245. The signal is sent to the GPIO entrance of EP4CE115F29. When receive the trigger signal, EP4CE115F29 capture the image. At the same time, with the interrupt trigger signal of ultrasonic, GPIO send a level signal of 3.3V, which switch to 24V by passing the level switching module, controlling the on-off of the relay. The hardware block of drive system is shown in Fig.2.

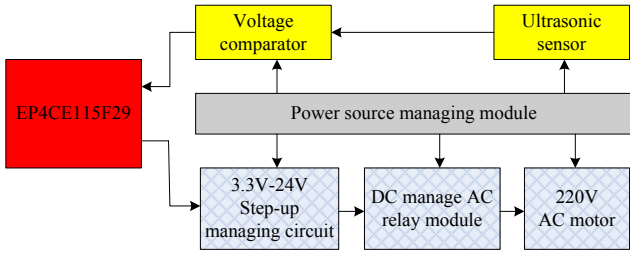


Fig.2 The block of transmission

The theory block of the image capturing and processing is shown in Fig.3. The PAL format analog signal which is exported from CMOS camera decoded with ADV7180, which produces Ycbr4:2:2 standard digital video data compatible to CCIR656, which includes horizontal synchronization, vertical synchronization and field synchronization. The Ycbr4:2:2 is sent to FPGA. FPGA switch the interlaced YCbCr 4:2:2 video signal and synchronizing signal to non- interlaced YCbCr 4:4:4 video signal and synchronizing signal. Then the gray image data formed by Y signal is processed with smoothing, threshold, recognition. The chromaticity space switching module switches the Ycbr to RGB video data, which is sent to VGA displayer. The VGA controlling module produces the individual VGA synchronizing signal including VGA_HS and VGA_VS, which makes the VGA displayer display the data.

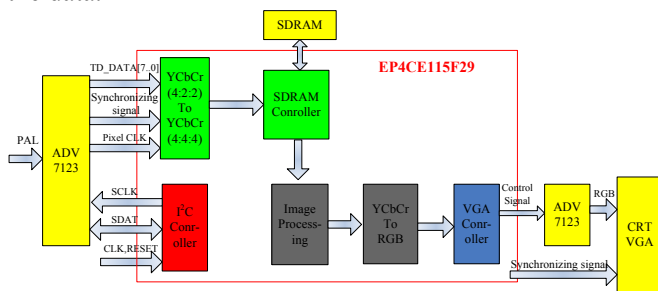


Fig.3 The theory block of capturing and processing image

III. THE THEORY OF DETECTION ARITHMETIC AND CARRYING IT OUT ON FPGA

The image captured is processed parallel and pipeline on FPGA. That include image smoothing and filtering,

ROI extracting, the detection of internal and external ring and the detection and cognition of stain. The procedure of detection arithmetic is shown in Fig.4.

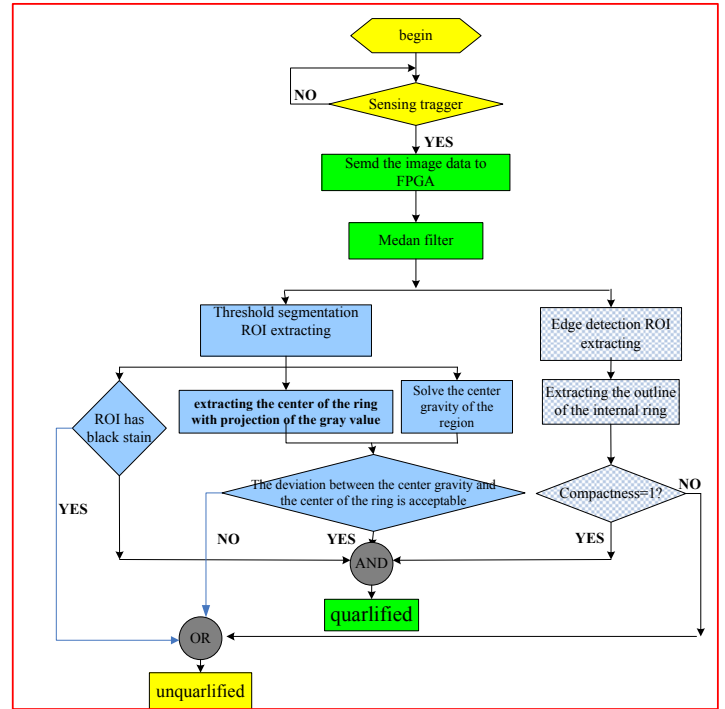


Fig.4 The procedure of the detection arithmetic

A. Median filter

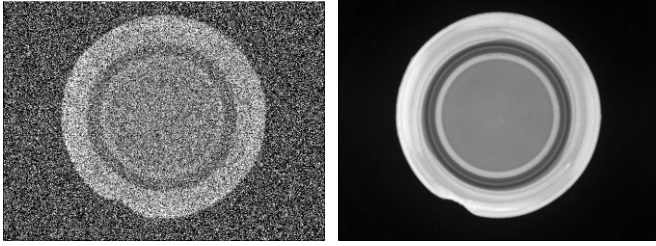
Gaussian filter is optimal smoothing filter, which filter the noise effectively and hold the sharp edge. Despite the smoothness of the filter is controlled with a parameter, the velocity of performing is low because of calculation of float, which make it complex carrying out on FPGA real time. Median filter is nonlinear filter based on statistical ranking, which also filter the noise but hold the sharpness of the edge. Though the smoothness can't be controlled with parameter, the velocity of carrying out is satisfied, which just need a clock period with the pipeline on FPGA. The expression is as follows.

$$g_{r,c} = \text{median}_{(i,j) \in W} f_{r-i,c-j} \quad (1)$$

$f(r,c)$ means the image before processing, $g(r,c)$ means the image after processing, and W is 3×3 mask

We use the macro feature module named Median filter 2D which is offered by Quartus II 10.0, in which we set the width of image as 640Pixels, the height as 480Pixels, and the deepness as 8Bits. We choose signal channel and the filter mask is 3×3 . The result is shown in Fig.5.(a) is the image with salt-pepper noise, and (b) is the image after median

filtering. What is shown is that the noise is filter effectively with the median filtering, and the sharp relatively edge is kept, which has major implication to the processing following.



(a) The image with salt-pepper noise (b) The image after median filtering

Fig.5 The result of median filtering

B. Threshold value segmentation, extracting ROI and distinguishing stain

We make the image that has been median filtered binary processing. After experimenting time after time, we conclude that the threshold of binary image is 8'd50, with which we can get the region of interest (ROI) of the bottle cap, shown as Fig.6. (a) is the image with stain before processing, and (b) is the ROI after threshold segmentation.

The extracted ROI take the run-length encoding method to save. The programming is shown in (c) of Fig.6. The minimum of every route includes the ordinates value and the abscissa value of the beginning and the ending of the route. Besides good to judging the stain, this method saves the memory space and improves the speed. We use a little RAM space to save the result. If the ordinates value is repeated in the result saved, we conclude that there is stain in the ROI. Then we mark the product under detection is unqualified, and separated by the rejecting device.



(a)Original image(b) The result of segmentation(c)The programming of route

Fig.6 The result of the threshold segmentation and the programming of route

C. external ring judging

If the ring is symmetrical, it's center gravity and the center of the ring is the same. We solve the coordinates of the center gravity and the center of the ring, and compare their deviation. Then we can know if the external ring has any defect. We conclude those products whose deviation is within 2 pixels to be qualified.

- 1) *extracting the center of the ring with the projection of gray value:*

The projection of gray value includes the projections of horizontal and vertical. The projection steps as follow: (1) initializing 2D array [10:0]Mem[0:M+N-1], mapping to a block in RAM. Mem[0: M-1] save the projection data of horizontal and Mem[M:M+N-1] save the projection data of vertical. The initialization is 0. (2) Going through the image T(r,c) which has been threshold segmentation. The horizontal projection saving unit Mem[r] is named after r. And Mem[M+c] is named after c. (3) The gray pixel of saving unit is 8'hFF. The saving unit is +1. (4) After being gone through, the memory units save the value of neighbor. (5) The coordinates of the center are ((C2-C1)/2, (R2-R1)/2). The horizontal projection of ROI shown in Fig.7 (b) is used to calculate the Y-axis, and the vertical projection is used to calculate the X-axis.



(a)ROI (b)the horizontal projection (c)the vertical projection

Fig.7 The result of the center of ring with the projection of gray value

2) *The center gravity of the region*

The center gravity is solved based on the ROI that has been extracted. The result of the ROI saved in the method of the route programming. We solve the area of the region with expression(2) easily. The symbol a in the expression (2) is the number of the stain in the region, which is equal to |R|. ce_i is the plotted value of the ending of the route, and cs_i is the beginning of route. The center gravity of the region is solved with expression (3) and (4).

$$a = |R| = \sum_{(r,c) \in R} 1 = \sum_{i=1}^n (ce_i - cs_i + 1) \quad (2)$$

$$n_{1,0} = \frac{1}{a} \sum_{(r,c) \in R} r \quad (3)$$

$$n_{0,1} = \frac{1}{a} \sum_{(r,c) \in R} c \quad (4)$$

D. The internal ring judging and carrying out the edge detection with Scharr on FPGA

We detect the defect of the internal ring with measurement of the region compactness. And the measurement of the compactness is solved with expression (5). The symbol l in the expression is the length of the outline of the region, and a means the area of the region, because of which we need to detect the edge, extracting the outline of the internal ring.

$$c = \begin{cases} 1, & \text{the region in the internal ring} \\ >1, & \text{the region out of the internal ring} \end{cases} \quad (5)$$

This system judge the products whose value of compactness is no bigger than 1.05 as qualified.

1) *The edge detection arithmetic named Scharr*

Sobel operator is an common edge detection operator. And its disadvantage is the accuracy in the approximate of derivative calculation in a small neighborhood such as 3*3. Scharr filter enjoy the same speed with Sobel filter, but is more accuracy. The block of Scharr edge detection arithmetic is shown in Fig.5. First we make the neighborhood and the Scharr operator a convolution calculation, getting the horizontal grads and vertical grads. Then by using the Euclidean norms $\|\nabla g\|_1 = |g_r| + |g_c|$, we get the grads value. Last judging the image edge with the threshold segmentation module and export the result of edge detection. With the neighborhood image data and the Scharr operator, we calculate the horizontal grads with expression (6) and vertical grads with expression (7). And we get the grads value with expression (8).

$$g_r = (3f_{31} + 10f_{32} + 3f_{33}) - (3f_{11} + 10f_{12} + 3f_{13}) \quad (6)$$

$$g_c = (3f_{13} + 10f_{23} + 3f_{33}) - (3f_{11} + 10f_{21} + 3f_{31}) \quad (7)$$

$$g_{r,c} = \begin{cases} 255 & , \|\nabla g\|_1 \geq T \\ 0 & , \|\nabla g\|_1 < T \end{cases} \quad (8)$$

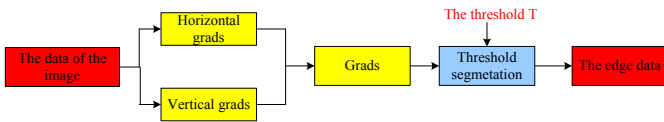


Fig.8 The block of the edge detection arithmetic

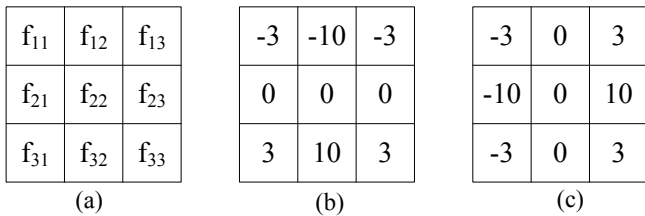


Fig.9 The 3*3 neighbourhood of the image and the Scharr operator

2) *Carrying out the Scharr edge detection on hardware*

The detection arithmetic refers to convolution and many multiplications and additions. The Scharr edge detection including window module, grads value calculation module and threshold segmentation module. To get the 3*3 window mask, we use the FIFO (First In First Out) module as the buffer of the image data, shown as Fig.10. FIFO which is instantiated by the M4K RAM module in FPGA produces row and column delayed signal. And we initialize the FIFO in the method of asynchronization resetting. When the data flows in, the image data of 3*3 keep changing, which makes the 3*3 mask process all the pixels. We convolute the masks with the programming multiplication adder and programming parallel adder module. The coefficient of mask is shown in Fig.11 (a). And (b) is the convolution of the image data after buffering with window module and mask. The inputs of programming multiplication adder adding or subtracting, then output. The circuit in (b) is packaged to a block. We get the grads value with parallel calculation after the instantiation and the modulation of mask coefficient. Then by passing the threshold, we get the edge outline.

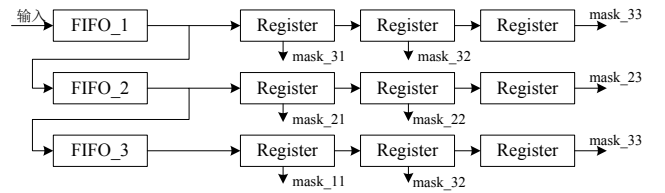


Fig.10 The module buffer

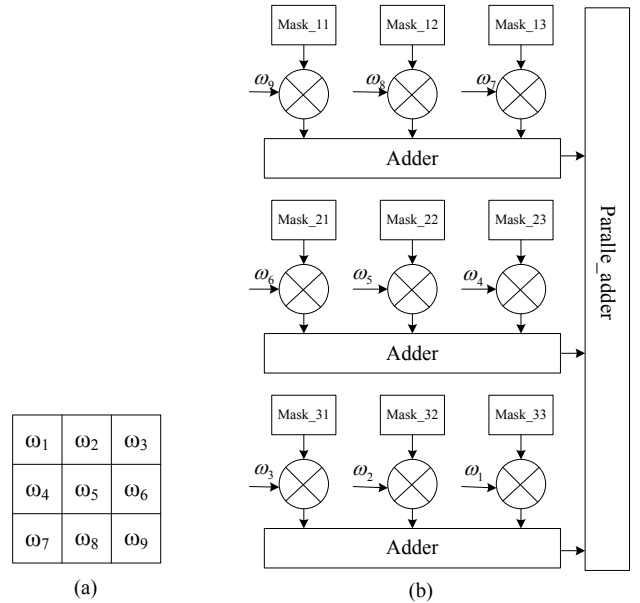


Fig.11 The theory of the convolution

IV. EXPERIMENTAL RESULTS

The hardware platform is shown in fig.12. The system includes something like light, ultrasonic transducer, CMOS camera, DE2-115, transmission, VGA displayer and so on.

The key link of the system is carrying out the arithmetic of image processing on FPGA.

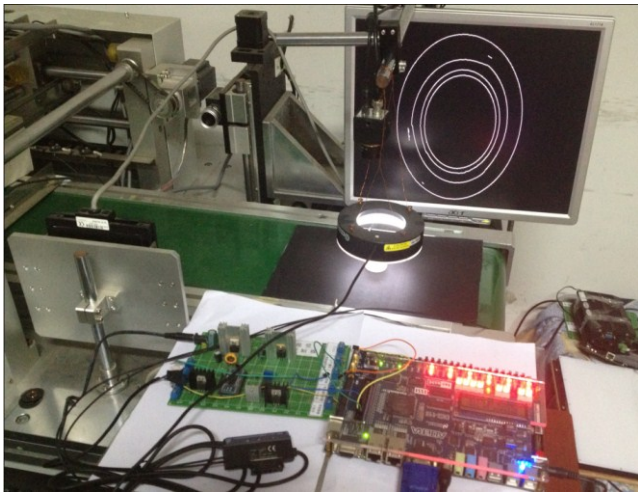


Fig.12 Hardware platform

The detection result of PET bottle cap is shown in Fig.13. Fig. (a) shows a qualified product. Fig.(b) shows the edge of the product in (a). Fig.(c) shows a disqualified product. Fig.(b) shows the edge of the product in (c). Seen from the images, the arithmetic can extract the edge of the target accurately. Because of the light, the edge extracted is being disturbed. However, with experimenting again and again, it's proved that the internal ring extracted with this arithmetic is accuracy. And we can conclude that the disturbing of light has no influence on the processing of the internal ring outline.

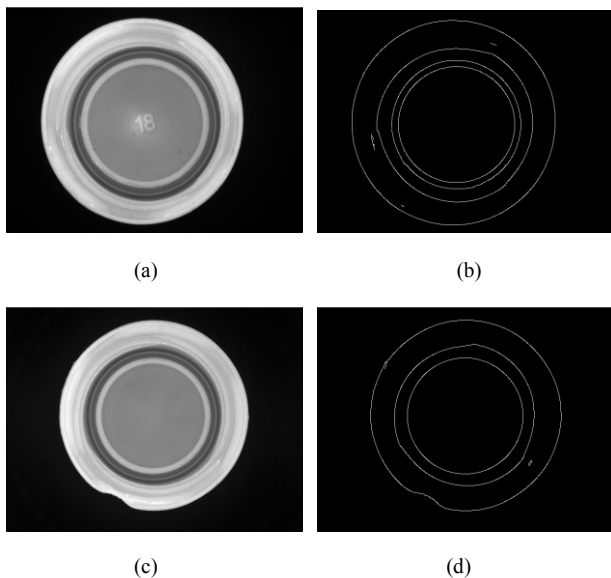


Fig.13 The result of the edge extracting

We experiment with 100 caps of 500ml Yibao mineral water bottle, including 5 caps damaged by man. The detection result is shown in Tab.1. The system would

not judge the qualified product as disqualified product. The detection accuracy rate is 98%, which meets the requirement of production line.

TABLE 1
THE RESULT of THE BOTTLE DEFECT DETECTION

| The number of tested | The number of qualified | The number of disqualified | The detection accuracy rate |
|----------------------|-------------------------|----------------------------|-----------------------------|
| 100 | 93 | 7 | 98% |

V. CONCLUSIONS

This system whose core processor is EP4CE115F29 capture and process image real time, and detect the defect of the PET bottle cap efficiently and accurately. Although the image processing arithmetic used in the system is easy to achieve in the engineering, and get the detection result accurately and efficiently, the system can't meet requirement of high-precision. To meet the harsh demand, it's necessary to look for more efficient ways. For example, making the Hough Transform work on the FPGA to get another online PET bottle cap detection system, which is faster, more accurately and has a higher precision.

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