Multi-channel Radio Spectrum Monitoring System

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Abstract— **As the radio signal has a large range bandwidth and is complicated, here a digital multi-channel monitoring system is designed. The system tunes the frequency of wide bandwidth radio signal via controlling the RF terminal, processing the baseband data by a variable bandwidth digital down conversion, finally, applying the digital processing algorithm to obtain the spectral information. Here four scan modes are designed to monitor the radio signal effectively from different angles. The software radio technology is applied so that the system can update efficiently without changing the hardware architecture. Finally, the spectrum processing result is demonstrated in the software.**

***Keywords*— Radio signal monitoring system; Software radio technology; Variable bandwidth digital down conversion; RF terminal; Multi-channel; Spectrum processing**

I. DESIGN SUMMARY

A. Design intention

With the rapid development of radio technology, the usage of spectrum resource is in a tense situation. Monitoring and managing of spectrum resource are particularly important, so it is meaningful for monitoring and managing the spectrum.
Today the digital software radio technology is becoming the mainstream of the development of wireless communication. In this context, a digital radio spectrum monitoring system is designed, which completes the tasks of radio spectrum monitoring and management efficiently though configuring the parameters of multiple scan modes.

B. Scope of application

The system monitors radio spectrum for civil task, military task, paramilitary monitoring task, investigation activity. It is also used for the receiver to analysis signal and spectrum and demand for analytical instrumentation technology.

C. Advantage of choosing Altera device

There is a rich variety of resource in FPGA, it enables the design system to achieve a very high throughput capacity via the parallel and pipeline technology. The modules of the system are highly configurable, thus they are flexible and efficient to parallel process the radio signals and to perform the multi-channel monitoring in real time, which is a general purpose processor platform could not achieve. Considering that the designed system requires mixing the quadrature baseband signal, variable bandwidth for filtering processing. The signal needs to compute FFT spectrum to analysis, calculating the amplitude, computing the average value and calculating the attenuation value. The cost of hardware resource is high, so using Stratix II family EP2S90F780I4 model chip to design the system.

II. FUNCTION DESCRIPTION

The block diagram of this system is shown in Fig 1. When the radio signal is received from the antenna, entering in the Radio Frequency(RF) terminal which is controlled by FPGA, and the processing data will be sent to computer. Finally, the result is demonstrated in the software.

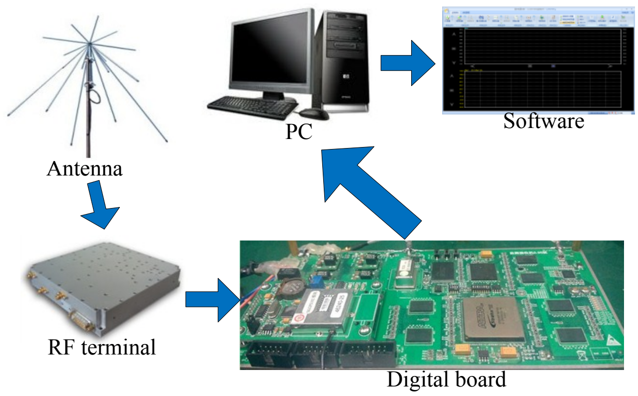

Fig 1 System diagram

The system monitors the radio signal mainly through the following several modes.

A. Multi-channel scan mode

Under multi-channel scan mode, system can display and monitor four channels at the same time. It is required to set the intermediate frequency and processing bandwidth of the four

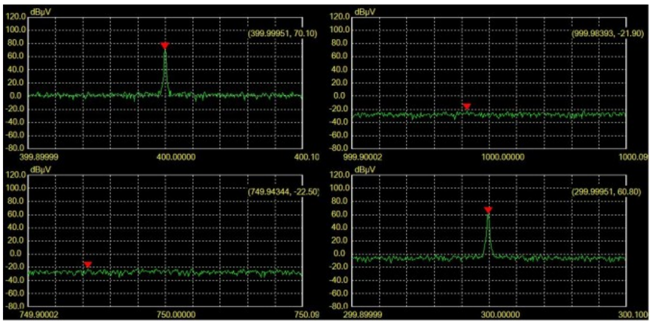

Fig 2 Multi-channel scan

channels before monitoring. Multi-channel scan mode is not parallel processing all these channels, but to monitor each channel with a millisecond time, sequentially monitored for the four channels. Monitoring result is shown in the following Fig 2.

B. Panoramic scan mode

System will monitor a range of frequency in the panoramic scan mode. Start frequency, end frequency and measurement resolution of the monitored frequency band will be set. The system will compute the processing bandwidth and the intermediate frequency according to parameters set before. The waterfall figure shows the probability of a signal that appears in the monitored frequency band. As depicted in Fig 3, the above is the panorama scan result of the monitored frequency band, and the waterfall figure is below it.

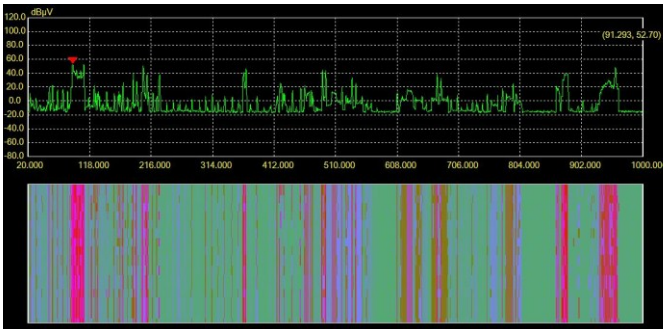

Fig 3 Panorama scan with waterfall

C. Search scan mode

Under the search scan mode, System requires presetting the parameters of multiple channels. The system will detect every channel according to the set detection threshold value to determine whether it dwells in the channel. It is depicted in Fig 4 when the system searches a signal in one of these presetting channels. The energy detection value is in the above, while the spectrum of monitoring signal is displayed below.

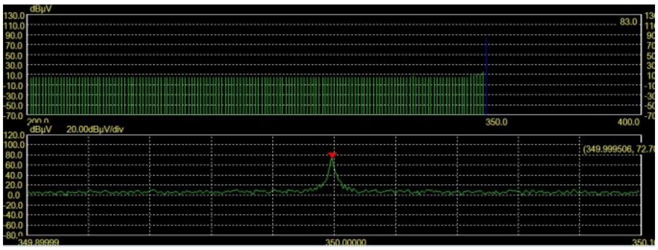

Fig 4 Search scan

D. Fix frequency mode

The system will monitor a single fix frequency in the fix frequency mode. The intermediate frequency and processing bandwidth are need to be set. The fixed frequency result is demonstrated in Fig 5.

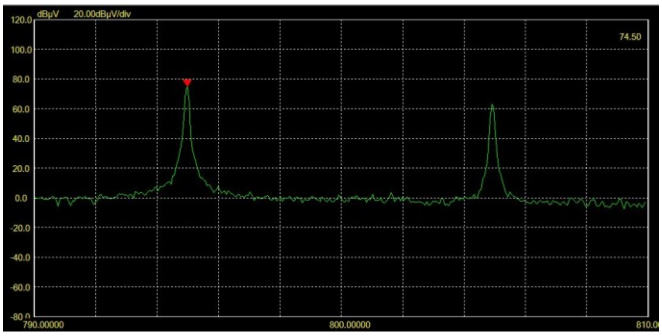

Fig 5 Fix frequency

III. Performance Parameters

A. System parameters

The system work frequency: 60MHz
Radio monitoring range scope: 20MHz-3.6GHz
Bandwidth: 17 kinds to choose range 1KHz to 20MHz
Spectrum Points: 512, 1024, 2048
Panoramic scanning speed: 5GHz/s
Search scan speed: 700 channel/s
The average number of spectrum: 1-16
Signal decimation: 1-512
Frequency measurement bias: 3Hz-71Hz
Image rejection ratio: >89dB
Third-order intercept point: >10dB
Phase Noise: (-111dBc/Hz) - (-96 dBc/Hz)

B. Hardware resource usage

Flow Status	Successful - Sat Jul 13 14:52:02 2013
Quartus II Version	9.1 Build 222 10/21/2009 SJ Full Version
Revision Name	Monitor_system
Top-level Entity Name	Monitor_system
Family	Stratix II
Device	EP2S90F780I4
Timing Models	Final
Met timing requirements	No
Logic utilization	85 %
Combinational ALUTs	39,392 / 72,768 (54 %)
Dedicated logic registers	46,954 / 72,768 (65 %)
Total registers	46954
Total pins	80 / 535 (15 %)
Total virtual pins	0
Total block memory bits	1,483,872 / 4,520,448 (33 %)
DSP block 9-bit elements	148 / 384 (39 %)
Total PLLs	2 / 6 (33 %)
Total DLLs	0 / 2 (0 %)

Fig 6 Hardware resource usage figure

IV. Design Structure

A. *Hardware design structure*

The structure of hardware system is following in Fig 7, it is concluding FPGA chip, RF terminal, ADC chip, DSP chip, clock chip, configuration chip, network interface and other parts.

RF terminal mainly tunes the signal received from antenna to a fixed 75MHz IF signal. The local oscillator frequency and the signal gain of the RF terminal are controlled and regulated by FPGA. The system clock is provided by the RF terminal, which is assigned to the clock chip and then sent to each module. ADC device samples the 75MHz IF signal outputting from RF terminal by the bandpass sampling method with a sampling rate of 60MHz.

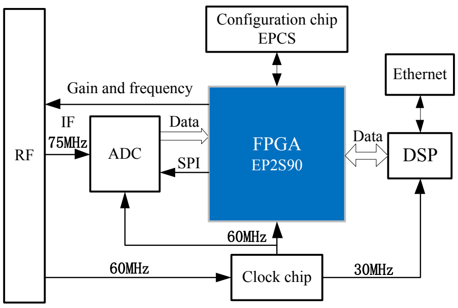

Fig 7 Hardware design structure

FPGA as the core, it mainly completes digital down conversion, filtering the baseband signal, processing the spectrum information and configuring the system parameters. As FPGA resource constrained the work could not use soft-core processor. Here DSP is selected to assist FPGA interact with the PC, completing the spectral data transmission.

B. *System structure*

The system sends the received configuration parameters to each module for updating when it works. Thereby, it can perform a variety of the monitoring tasks. In the signal processing section, the signal accesses to the system in two paths. It goes through the digital automatic gain control (DAGC) to adjust the RF terminal to control the IF signal amplitude in one path, it goes through the variable bandwidth digital down conversion module and FFT spectrum analysis module in another path. Finally, the spectrum processing data is sent to the computer, drawn into the software to be intuitive for the user to observe and analyse.

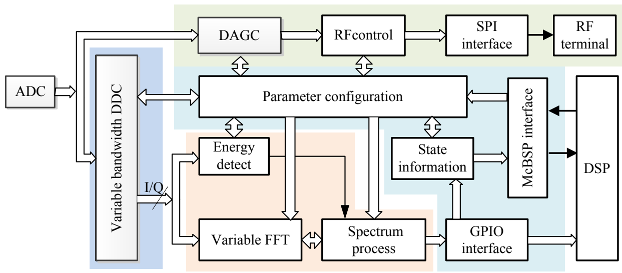

Fig 8 System structure Block Diagram

C. *RF terminal control structure*

Frequency terminal control module consists of the digital automatic gain control (DAGC) and a tuning frequency configuration control. DAGC plays a role in stable of the input signal, the IF signal which sampled by the ADC is calculated the gain to adjustment the RF terminal all the time. The tuning frequency is obtained by the configuration parameter, and the tune frequency is range from 20MHz to 3.6GHz. All the tuning frequency signals via the RF terminal are fixed IF signal with frequency 75MHz, bandwidth 20MHz. The RF terminal control structure is shown in Fig 9.

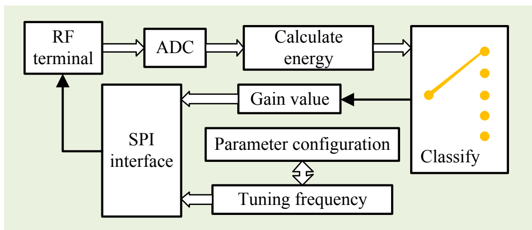

Fig 9 RF terminal control structure

D. *Variable-bandwidth digital down conversion structure (VBDDC)*

When the IF signal flows in FPGA after outputted from RF terminal, then digital down conversion processing will be conducted. It needs to implement a variety of different bandwidths flexibility and to process signal efficiently when monitoring the radio signal spectrum. It takes the parameter configuration mode in real time to update the processing system, getting the baseband data that meets the desirable. Its implementation structure is as following in Fig 10.

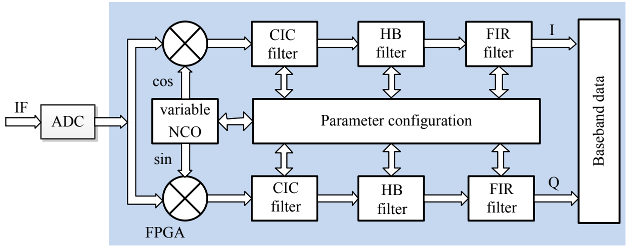

Fig 10 Variable bandwidth digital down conversion implementation structure

E. Spectrum processing structure

Spectrum processing part fulfils the FFT transformation and the average of the baseband signal, windowing the spectrum, calculating the modulus value, calculating the attenuation spectrum processing, etc. Realization block diagram as shown in Fig 11Fig 11, Most of these function are implemented by the IP cores of Altera.

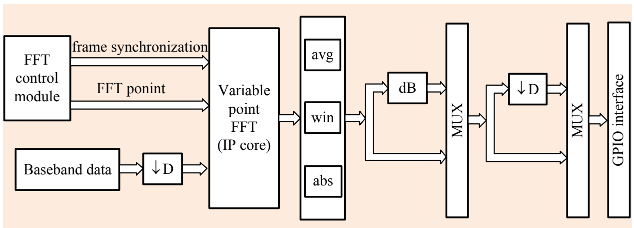

Fig 11 Spectrum processing implementation structure

F. Communications interface structure

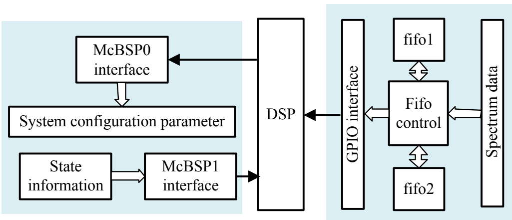

Fig 12 Communications interface structure

Interface is mainly composed of McBSP interface and GPIO interface. McBSP interface is responsible for the system configuration parameters, and returning the system working status information. GPIO interface is used to transmit the system processing spectral data. Communications interface structure is shown in Fig 12.

V. DESIGN METHOD

A. Configuration Parameters

The best feature of the radio spectrum monitoring system is the way to update the entire hardware system in real time by taking software radio technology. It fulfils different tasks conversion by configuring the parameters. Here McBSP0 interface is taken by transferring corresponding configuration parameters. It sends the address of the instruction and the instruction parameter in the cross form as a communication protocol, such as instruction address, instruction parameter, instruction address, instruction parameter, instruction address, instruction parameter. It cyclically sends all the instruction address and instruction parameter in this way, and sending the final termination instruction at the end. Instruction processing flow as shown in Fig 13, it first identifies if the instruction is an instruction address or an instruction parameter, and it registers the configuration parameters according to the corresponding situation. If a finish instruction is received, it will configure and update all system parameters.

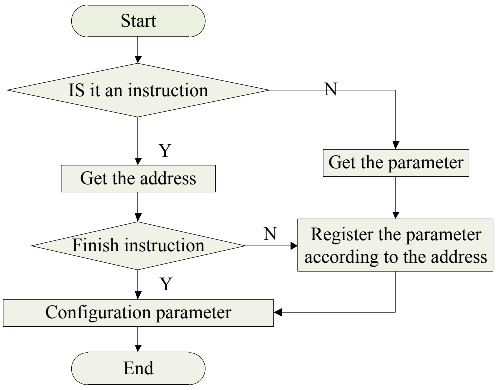

Fig 13 Parameter instruction processing flow

B. RF terminal control flow

1) Implementation flow diagram

DAGC control of the RF terminal flow implementation is shown in Fig 14. It first calculates the baseband data power estimation, comparing the estimated value with the set reference value. Then adjustment and controlling the gain value of the RF terminal according to the comparison result. The tuning frequency is determined by the configuration parameter, it just is obtained from the parsing instruction. Finally, DAGC value and the tuning frequency parameter together are sent to the RF terminals via the serial SPI interface, fulfilling the control of the RF terminal.

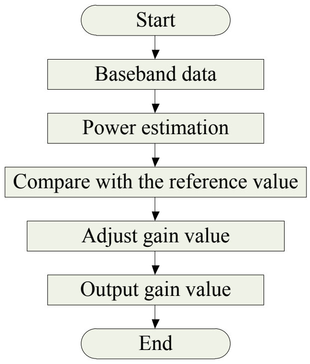

Fig 14 DAGC control flow

2) Power estimation

Power estimation is calculated from baseband data in real time. Fig 15 shows the function block diagram of power estimation. At first, envelope detection module obtains the envelope of the signal by calculating the absolute value of the baseband data. The average amplitude is got by multiplying and accumulating a frame of the baseband data. The average amplitude will be converted into average power in dBm unit at last.

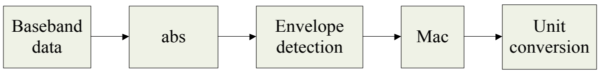

Fig 15 Power estimation

3) *Adjust gain value*

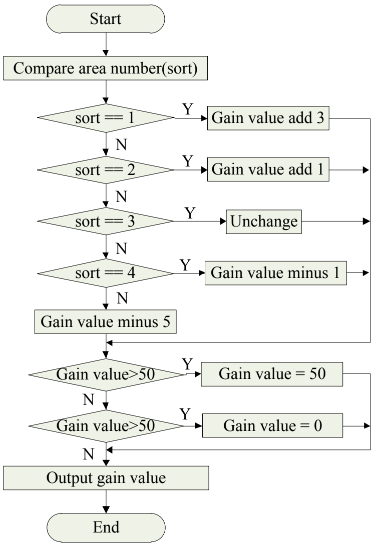

Fig 16 Adjust gain value

Power estimation result is used for comparing with a reference value. The reference value is classified into four intervals which range from 0dBm to 50dBm. Gain value is dynamically regulated according to the actual power, so the power of intermediate frequency signal outputted from RF terminal keeps stable. The process of adjustment is shown in Fig 16, it dynamically adjusts the gain value, so the RF terminal will output IF signal power which remains stable.

When the RF terminal works, the configuration parameter is shown in table I. the designated instruction address is 102, the lowest 23 bits of instruction parameter represent the tuning frequency which ranges from 20 MHZ to 3.6 GHz. The minimum unit is 1 KHZ, and minimum effective step is 125 KHZ.

TABLE I

Num	Command	Address	parameter
1	RF_word	16'h102	RF_word[22:0]

C. *The implementation of the variable bandwidth digital down conversion*

DDC is the key part in the IF signals processing, here it mainly consists of three parts, digital voltage controlled oscillator (NCO), cascade integrator comb (CIC) filter, finite impulse response (FIR) filter. Here the designed variable bandwidth DDC can achieve 17 different filter bandwidths through configuring the parameters of the local quadrature mixer oscillator frequency.

1) *NCO*

Here NCO is implemented by the IP core, just setting some parameters, the NCO can quickly be integrated into the systems engineering. The system clock is default as 60MHz, the output of the oscillator signal is default as 15MHz. Considering resources and ensuring the spurious free dynamic range(SFDR) to meet the requirements of the case, here setting the Multiplier-Based approach to implement NCO. Because there will be some cut position to implement NCO, it needs to add the dither to compensate for the noise generated by the truncation. As the output frequency changing, a compromise intermediate position Dither Level should be considered. In order to achieve the purpose of changing the local oscillator frequency, it needs to activate the Frequency Modulation Input Option. As the system needs quadrature signal, two output signals option is required. It only needs to configure the parameters of frequency control word to realize the variable local oscillator frequency when the system works. The NCO output signal of the oscillator multiplies with the digital IF signal that is sampled by ADC When it performs the mixing frequency, as shown in Fig 10 above.

2) *CIC filter*

CIC filter contains the integration, the decimation and the differential, processing flow as shown in Fig 17. Integral and differential both have 5 stages to cascade. Decimation part is performed by a loop counter in FPGA. The number of decimation is the counting period. When the count is 0-(D-2), the system is on hold, while it is the activation sample status when the count is (D-1). The output rate will be reduced to the input rate of 1 / D times, the number D is from the decimation configuration parameter.

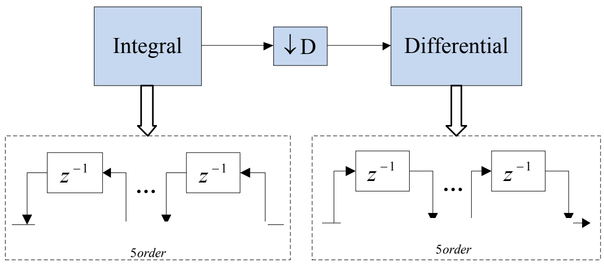

Fig 17 CIC filter process block

In order to cascade with the FIR filter, it needs to truncate the data. Because there is a high gain from CIC filter, normal truncation will cause the significant bits are all rounded. So it requires the barrel shifter to pre-shift the data. According to the reference literature, the shift value is shown below.

$$shift = floor[60 - \log_2(D^5)] \tag{1}$$

The shift value is calculated based on the extracted value D first, then updating the system by the configuration parameters.

3) FIR filter

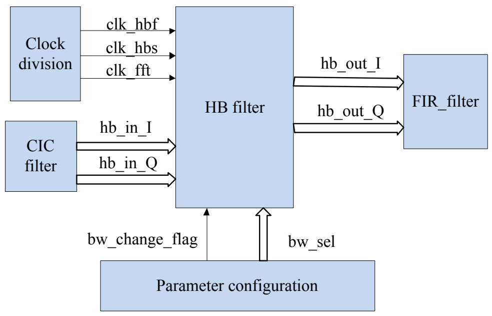

Fig 18 HB filter

FIR filters contain HB filter and FIR sharping filter. HB filter is the second stage filter after CIC filter, and FIR filter is the third stage filter. The structure is shown in Fig 18. HB filter is a decimation filter which the factor is 2, with this feature it can save more than half resource compared with normal FIR filters. Here they are implemented by calling the IP cores which are provided by ALTERA. Through the configuration module, different set coefficients need to be

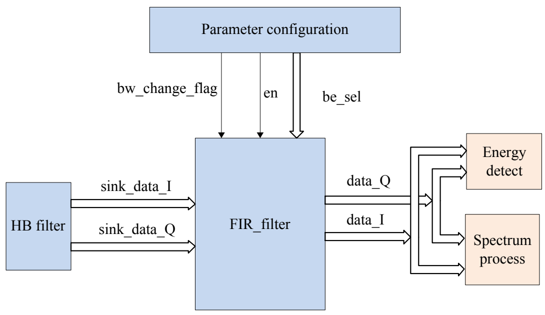

Fig 19 FIR filter

selected applied to the HB filter and then achieve 17 kinds of bandwidth combined with CIC filter and FIR sharping filter.

FIR filter is the last stage filter, which is implemented by calling the IP core too. Similar to HB filter, it can achieve 17 kinds of bandwidth by choosing the coefficients. And its I/O interface is shown in Fig 19.

The processing flow starts with applying HB filter or FIR filter, then changing the coefficients according to the bandwidth, it generates the configure done signal at last, the filter processing flow is shown in Fig 20.

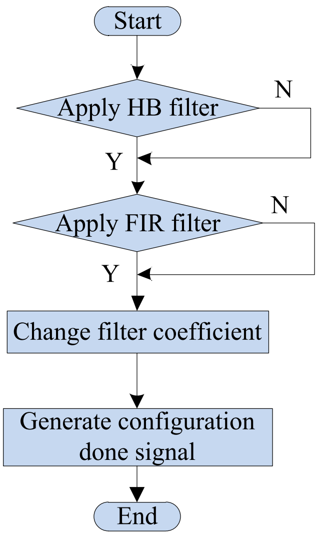

Fig 20 Filter processing flow

4) Divide the clock

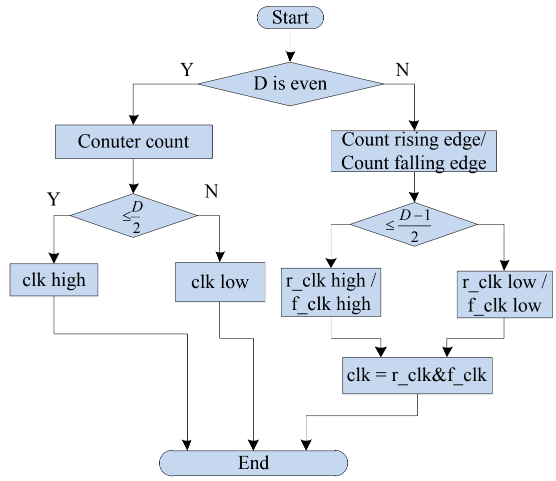

Fig 21 Clock divider processing flow

As the decimation factor is variable and there are three stages filters, the data rate of different stage is variable, so they are in different clock domain. Clock period is changed with the corresponding bandwidth. Noting that the PLL can only get stationary clock period, we have to design a clock divider module to perform variable clock period. Its processing flow is shown in Fig 21. When the decimation factor D is even, the clock divider which is symbol as clk_D goes high when the counter is lower than D/2, clk_D goes low when the counter large than D/2. When the decimation factor is odd, we need two counters respectively, one counter counts for the rising edge of original clock and the other counts for the falling edge. Then we process the r_clk and the f_clk by using and logic, finally, we get the desired clock, clk.

5) Configuration parameter table

TABLE II

Num	Command	Address	parameter
2	CIC_para	16’h200	CIC_shift[24:18]
			CIC_D[17: 5]
			BW_DDC[4:0]

This part of the system needs to configure three parameters, CIC_shift parameter is used as the CIC filter barrel shifter, CIC_D is used as the CIC Decimation filter coefficients, BW_DDC is the code number of corresponding FIR filter coefficient.

D. Spectrum processing

1) Variable Point FFT control module

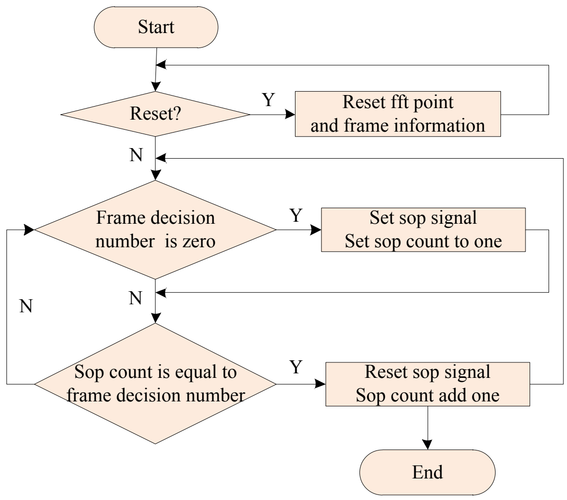

Fig 22 FFT control module

Variable point FFT module is performed by calling FFT core function. Here the variable streaming structure is selected. The structure allows a continuous input data stream, the main control signals of the FFT module are frame start operation (sop), frame end operation (eop) and data valid. In order to control the baseband rate, you need to configure a frame decimation parameter, the number of every frame data is the number configured by FFT points. The control module implementation processing is demonstrated in Fig 22.

2) Spectral smooth processing

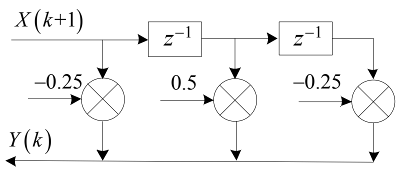

Fig 23 Spectrum windowing flow graph structure

The spectral smoothing mainly windows the spectrum in frequency domain, calculating the modulo value, calculating the average value and other processing. Frequency domain windowing is derived from time domain windowing formula, here chosen hanning window, derivation equation is shown as following.

$$Y(k) = 0.5X(k) - 0.25X(k-1) - 0.25X(k+1) \qquad (2)$$

The equation represents the spectral data after adding window. The implementation structure of windowed stream is shown in Fig 23 below.

It calculates modulo value of the spectrum after windowing, the step is fulfilled by multiplying and adding the real part and imagine part of the spectral data. The final step is to realize the spectral smooth by averaging several frames spectral data. Spectral averaging processing flow is shown in Fig 24. The number needs to average is configured by the configuration parameter, and then it is registered in the avg_N signal. And accumulating the spectral data in unit of frame, it outputs the average result when the accumulated number is the same as configuration parameter.

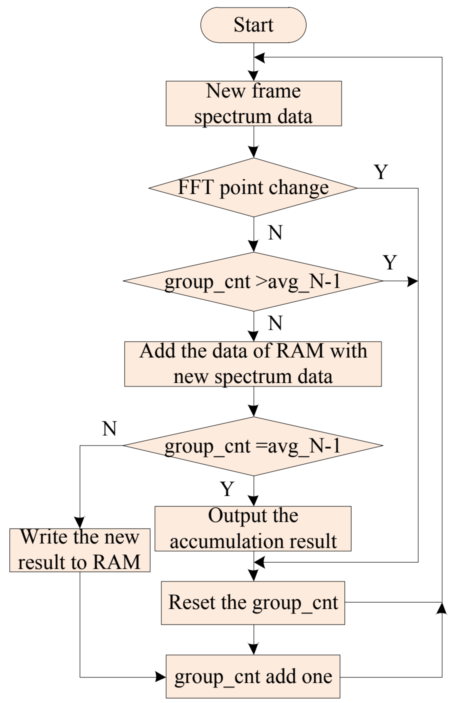

Fig 24 Spectral average processing flow

3) Spectrum logarithmic processing

This part of the spectrum data needs to have a logarithmic operation in order to visually display the scan result on the computer. Since the IP core has to seek nuclear based on the natural logarithm, it needs to be convented to the base-10 logarithm logarithmic. According to changing base equation, the result requires multiplying a constant to compensate. This part of the processing diagram, as shown in Fig 25, the float-fixed point module and the fixed-to-float point module are both implemented by the IP cores, the multiplier is using the fixed point multiplier to perform the multiplication operation.

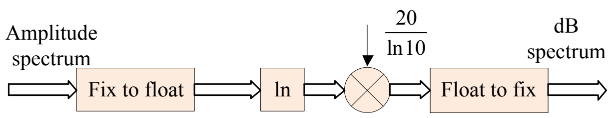

Fig 25 Spectrum arithmetic processing block diagram

4) Frequency decimation processing

Panoramic scan mode requires scanning multiple channels all the time. Therefore it selects the largest selected N data from each frame spectrum and then groups these data together into a new frame, finally, the result is displayed on the computer. So the frequency spectrum data decimation processing is required, also the position of selected data is required to calculate the detail frequency. The processing block diagram of the data decimation is as shown in Fig 26.

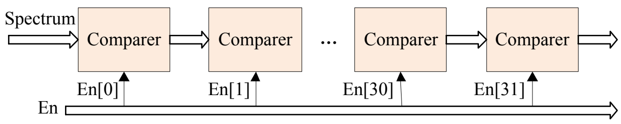

Fig 26 Comparator structure

Each comparator unit works such as Fig 27, when the spectral data flows into these comparators, the comparator compares the new input spectral data with the last remaining larger data, and sending the smaller one to the next stage. Each frame data will leave up to 32 biggest data, and the position of these data will be recorded. In order to calculate the frequency of these data, the position of these data also requires adjusting, but from small to large, relatively the same way.

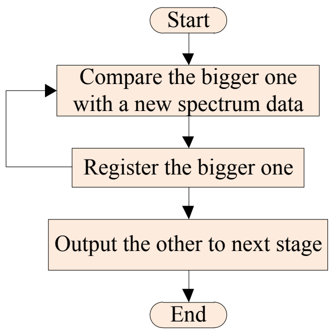

Fig 27 Comparator unit processing flow

5) Energy Detection

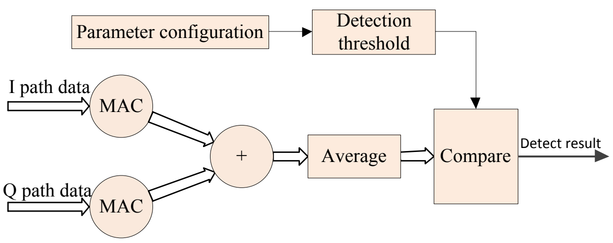

Fig 28 Energy detection processing

Search mode needs to detect the energy of baseband data, and comparing with the configuration detection threshold parameter to decide whether to reside in the channel. The system detects the energy of the baseband data in every configuring channel, the detection processing as shown in Fig 28.

6) Configuration Parameter Table

TABLE III

Num	Command	Address	parameter
3	fft_para	16'h300	fftpt[29:18]
			dB_en[17]
			aver_N(16:9)
			deci_N[8:0]
4	ED_para	16'h400	Hold_time[5:0]
			Threshold[15:0]

There are two configuration instructions. A configuration instruction is used to configure the FFT spectrum processing, FFT points and the spectrum data type (dB/abs), the number of frames to average and the number for spectrum data to decimation. Another instruction is to configure the energy detection threshold and reside time after detect effectively. The unit of residing time is second and is performed by dividing the system clock time.

E. Communication Interface

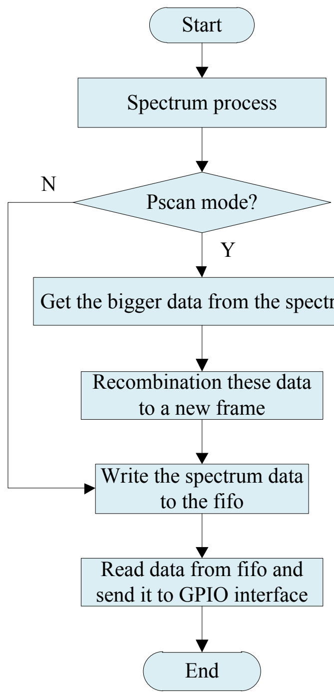

Fig 29 GPIO interface design block

1) McBSP interface

Here has two McBSP interface, McBSP0 and McBSP1. McBSP0 is used for transmitting data for the system configuration parameters. McBSP1 is used for sending the status information of the system. In order to communicate convenient, the transferring clock and frame synchronization signal of the interfaces are generated by FPGA.

2) GPIO interface

GPIO interface is used for transmitting the processing spectral data after scanning. Because the panoramic scan mode requires regrouping the spectrum decimation data from to new frame data, while the spectral data of other scan modes can be directly exported via GPIO interface, the design processing is shown in Fig 29.

F. Scan Mode Design

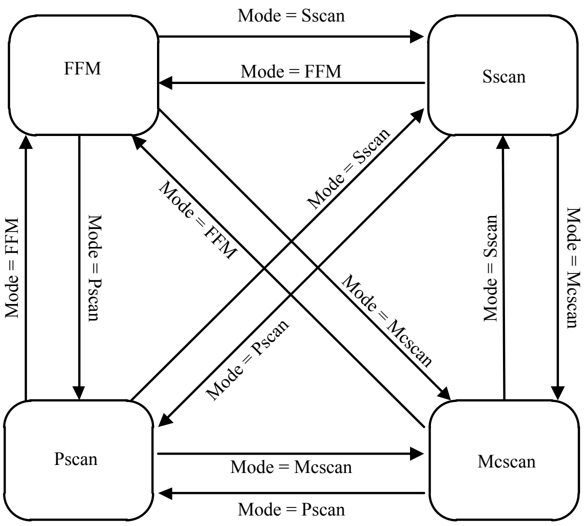

Fig 30 Mode switching diagram

1) Multi-channel scan mode （Mcscan）

Multi-channel scan mode is performed by setting four channels with a short scan cycle for every channel, and it can easily carry out on monitoring the four channels in real time.

2) Panoramic scan mode（Pscan）

Panoramic scan mode is a coarse frequency scan which can intuitively demonstrate a large range of the radio signal that is monitored. In order to display in real time, it needs to select the largest spectrum data from each frame spectrum data, so the rate of the spectrum data is slowed down.

3) Search scan mode(Sscan)

This mode detects the signal for a series of stored channels, if a signal is detected, then the system dwells in the channel with a configurable dwell time.

4) Fix frequency mode(FFM)

Fix frequency mode is monitoring a fixed channel, and it can monitor a selected frequency which ranges from 20MHz to 3.6GHz with 17 different bandwidths.

5) Switching the mode

Several working modes require mutual switching when monitoring the signal in real time, and the switching process is depicted in Fig 30.

G. DSP configuration parameter and data transmitting

In order to configure and transmit the processing spectral data in real time, here applying DSP to perform managing and scheduling the multiple threads through the BIOS. FPGA is configured through McBSP0 interface, FPGA sends the state information by McBSP1 interface, system processing spectral data is transmitted via GPIO interface.

VI. DESIGN FEATURE

A. High practical and commercial value

This designed system is applied for civil, paramilitary and military monitoring tasks, as well as radio spectrum monitoring investigation business, analysing for the receiver and analytical instrument of spectrum and signal. Because it has a wide range of applications, it has a high practical and commercial value.

B. Self-designed multi-scan mode

As the bandwidth range of the radio signal is wide and dynamic range of the radio signal is large, the designed system can monitor all the channels effectively though the four scan modes.

C. Supporting multiple bandwidths digital down converter

Comparison with the traditional digital down conversion, this system can select a variety of local oscillator frequency and switching filter by configuring the system parameters, the bandwidth of IF signal ranges from 1KHz to 20MHz and has 17 kinds of selection.

D. Excellent user Interface

The system independently develops an excellent interactive interface, and shows the monitoring results of various modes on computer, greatly simplifying the debugging task.

E. Designing the hardware independently

According to the functional requirement of the radio spectrum monitoring system, as well as the cost factor, the hardware circuit is designed to match these requirements. RF terminal, ADC device and communications interface form a completing network for transmitting data. The usage of FPGA chip provides a good hardware support for the entire system and digital signal processing algorithm.

F. Easy to expand and upgrade

Since the system of FPGA-based embedded system has the software programmable feature, the designed system applies the software radio technology, which can flexibly and easily update the system without changing the hardware circuit.

VII. CONCLUSIONS

Altera's FPGA chip provides many common IP cores which make the design work easier and more flexible for the system, greatly enhance the design schedule. The system uses software radio technology, which can update online without changing the hardware architecture and efficiently achieve the goal of monitoring the radio signal in real time. For a large bandwidth radio signal, the system tunes the frequency of the radio signal via controlling the RF terminal, so it is converted into a fixed frequency IF signal, the system obtains the time domain baseband data by applying the variable bandwidth digital conversion to process the IF signal, then processing the baseband data via digital signal processing algorithm. In order to visually demonstrate the result, the spectral processing data is sent to computer, thus secondary treatment of the result by drawing the result in the software which is specific designed. The monitoring mission is fulfilled through the designed multiple scan mode, the result effectively reflects the entire monitored frequency band. However, the system still has some shortcomings, such as it needs to obtain a higher SFDR when the NCO changes dynamically in variable bandwidth processing section. A better compensate for the loss of frequency and power consumption is required in spectrum processing part of the system. The rate of transmitting data is not high enough in transfer interface section, thus a better way should be taken to improve the system performance.

ACKNOWLEDGMENT

I would like to thank one and all who helped us to successfully finish this system. I am indeed grateful to Mr. Wei Xia for helping me reviewing the document and providing valuable feedback and comments.

This work is supported in part by National Natural Science Foundation of China (Grant NO. 61101173), the Fundamental Research Funds for the Central Universities (Grant NO. ZYGX2010J020).

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