

A Lane Departure Warning System Based on Monocular Vision

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Abstract— This paper introduces a monocular-vision-based lane departure warning system. Based on a fast lane departure warning robust algorithm and the NIOS II of Cyclone IIFPGA as the core processor, this system can achieve the lane line detection effectively. The software and the hardware of the system are designed with the aid of the Avalon bus for customizing the IP core. Test results illustrate that both the accuracy and real-time performance of this system satisfy the demand of all-weather lane departure warning, and thus enable safe driving.

Keywords— lane departure; FPGA; lane line detection; monocular-vision

I. INTRODUCTION

The lane departure caused by the fatigue and negligence of drivers result in a lot of serious traffic accidents, and the proportion of such traffic accidents is increasing year by year(e.g. [1]-[3]). In order to prevent lane departure accidents, extensive research on the LDWS (Lane Departure Warning System) has been carried out. At present, the lane line detection often uses the machine-vision recognition method, including feature recognition and model recognition(e.g. [4]), where the former is widely used. However, it fails when there is shadow on the road or there are some damages of the lane line edge. The latter can effectively overcome the external environment influence, such as road pollution, shadow, and poor illumination and so on. Due to the complexity of the external environment, however, mistake appears during identification.

LDWS has the characteristic of high real-time requirements and complex running environment. Because of the great uncertainty and diversity of the road conditions, LDWS needs to use a variety of complex processing algorithm in order to improve the accuracy of the lane line detection(e.g. [5]-[8]). This paper mainly focuses on the monocular vision identification. Based on a specialized designed fast lane line detection algorithm, the LDWS is realized is achieved on Altera DE2 FPGA platform.

II. BUILDING THE PROTOTYPE SYSTEM FOR LDWS DESIGN

This LDWS uses Cyclone II as the CPU, and uses ADV7181 for image capture. The captured image will be stored in the SRAM for the FPGA to compute. When lane departure happens, the buzzer will send alarm.

In order to make full use of the parallel processing features of FPGA, and combine with the flexibility of FPGA hardware and software, this design built a SOPC system on

DE2. Hardcore firmware is adopted to realize the image processing algorithm, and NIOS II is adopted to complete the control function, whose processing speed requirement is not high. This cooperation between hardcore and NIOS II made the LDWS more flexible. The system is designed as follow:

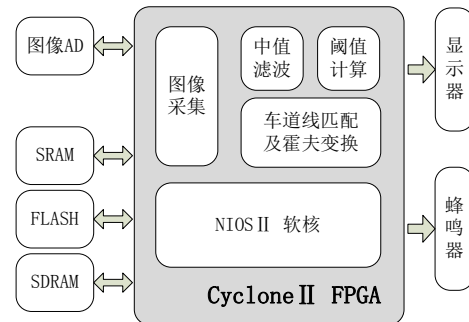


Fig 1 The structure of system

Avalon bus is a kind of ideal system inline bus between the processor and peripherals and it can be automatically generated by the SOPC Builder. Median filter, thresholding, lane line matching and Hough transform are all designed the IP core based on the Avalon bus. Avalon bus generated by the SOPC builder is as follows:

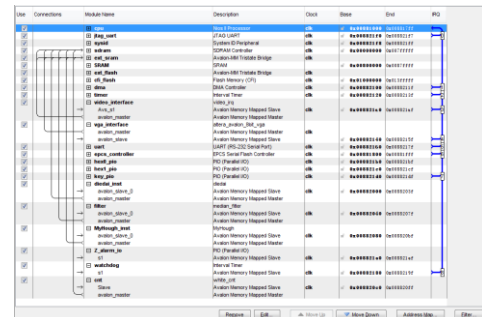


Fig 2 Structure of SOPC

The figure below shows the report for the resource utility of our design based on DE2.

Quartus II Version	8.0 Build 215 05/29/2008 SJ Full Version
Revision Name	sopc_de2
Top-Level Entity Name	sopc_de2
Family	Cyclone II
Device	EP2K35F67206
Timing Models	Final
Net timing requirements	No
Total logic elements	14,921 / 33,216 (45 %)
Total combinational functions	11,774 / 33,216 (35 %)
Dedicated logic registers	7,570 / 33,216 (23 %)
Total registers	7743
Total pins	189 / 475 (40 %)
Total virtual pins	0
Total memory bits	159,232 / 483,840 (33 %)
Embedded Multiplier 9-bit elements	12 / 70 (17 %)
Total PLLs	1 / 4 (25 %)

Fig 3 Resource consumption of the system

III. THE DETECTION ALGORITHM FOR LDWS

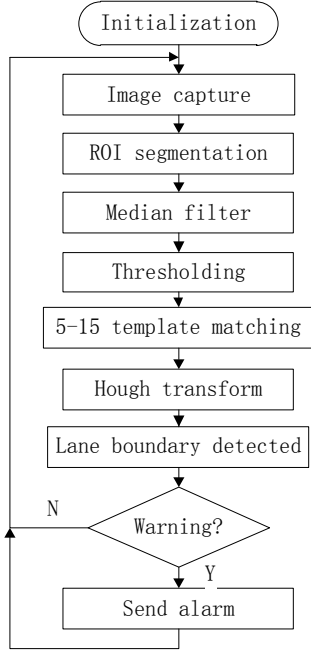


Fig 4 Lane departure detection algorithm

A. ROI SEGMENTATION

Through the analog camera, the 640*480 video images of the road can be captured. After video decoding, the brightness signal of the video images is the gray images of interest. The ROI (Region of Interest) is the part of lane line that we are interested. In order to reduce the calculation and improve the processing speed, the ROI is divided into two 160*160 rectangular areas for pretreatment.

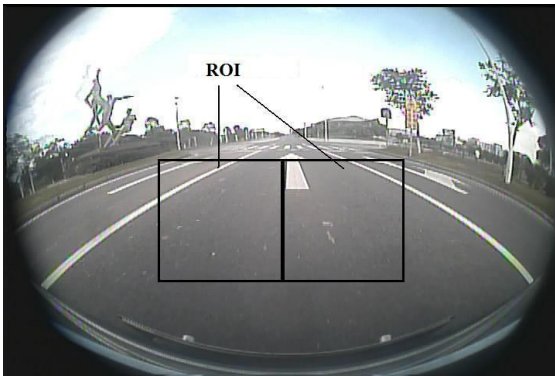


Fig 5 Divisions of the image

B. Median filter

The 3*3 window median filtering algorithm uses FIFO (First Input First Output) buffer for reading 9 pixel data at the same time. After median filtering arithmetic, the next 9 pixel data will be done with the same filter until all data in the ROI has been done. Median filter can reduce the noise produced by image capture and transmission.

C. Thresholding

Binary threshold calculation circuit adopts the method of

image gray level distribution. In order to eliminate the impact of glitches raised by the complex road conditions on the curve of grayscale distribution, we use the following steps. First, the gray space was divided into 16 identical space steps, and the gray histograms of the 16 identical space steps were stored in 16 registers. Second, based on the Avalon bus, the gray values of 4 pixels were for gray histogram statistics every time. Third, using iterative method calculate the threshold. The feedback of threshold to NIOS II is transformed by Avalon bus.

D. 5-15 template matching

After image pretreatment, the effect of binarization is relatively good. In order to further reduce the system operation time, the transverse detection was designed with the line space of 5 pixels. Based on the width feature of lane line, a 5-15 template matching algorithm was used in lane line matching. First, a max value and a min value should be set as the width matching threshold of lane line. According to the width specification of lane line and the experimental data, the max and the min are set to 5 and 15, respectively. Then analyze the images, to find the centerline of the lane line. The coordinate of the center is stored in a new register.

E. Hough transform and ultra-line judgment

Hough transform has strong robustness, and is suitable for lane line detection. The Hough transform circuit adopts double channels parallel processing method, where the parallel matching the coordinates of the left lane line and the right lane line can significantly reduce the time of computation.

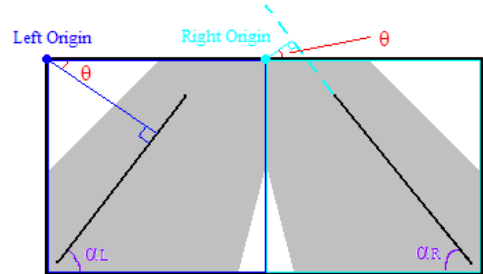


Fig 6 Hough Transform

IV. SYSTEM TEST

As for different road conditions, the system can accurately identify the environmental situation when the vehicles cross the line. Due to the use of the lane line matching algorithm, we effectively eliminate the effects of the pavement marking, night lighting on the lane line identification. In the computing environment, single static image can be processed in about 19 ms and video data per frame is in approximately 24 ms. Detailed results that the processing time of system under different road conditions are shown in the table below, fully meeting the requirements of real-time.

TABLE I
VIDEO PROCESSING RESULTS

Video project	Total frames	Number of Warning	Number of Error	Accuracy (%)	Consuming per frame(ms)
Daytime	7939	17	0	100	22.702
Evening	2431	10	1	90	24.770
Night	6387	12	1	92	23.501

V. CONCLUSION

The LDWS introduced in this paper is designed based on the monocular vision and successfully realized on Altera DE2 FPGA platform. The LDWS can accurately identify the lane departure in different road conditions, and thus enable a reduction in traffic accidents caused by lane departure.

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