Galaxian Game on Altera DE2-115 FPGA Architecture

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Abstract— **With the development of computer and network technology, the pace of people's life is much faster. At the same time, the need for entertainment is also growing. The game based on handheld devices is becoming more and more popular. It has been booming along due to its educational, fun, casual, easy to carry, easy to operate, highly interactive and many other features to meet the people's entertainment needs. This paper introduces the embedded systems based on general-purpose software development model and development process, including the design of hardware platform and software. The design of the hardware platform is based on the Altera's DE2-115 Series development board, the software platform is Nios II EDS 10.1 and the programming language is C and VHDL. Based on the SOPC tool, we designed the reconfigurable IP cores of the VGA display, LTM touch screen. With Galaxian game as an example, we design a embedded game based on GUI. The results show that the game system is human-computer interaction friendly and it has quick response and action. This configurable IP core has high flexibility, variability, plasticity and it can achieve more functional expansion and development with the same resource.**

Keywords— **Configurable IP core; DE2-115; FPGA; SOPC; hardware/software co-design**

I. INTRODUCTION

With the development of SOC (System on Chip) technology, many companies have put embedded processor core on their own ASIC (Application Specific Integrated Circuit) chip to build a system, in which the ARM processor kernel has more users. Two vendors Altera and Xilinx also put hard-core ARM and Power PC on their own FPGA (Field-Programmable Gate Array) chips.

Nios is of low-end embedded CPU soft cores developed by Altera Corporation and which can be used in almost all the internal FPGA of Altera series. Because Nios processor and peripherals are designed with HDL language, and making use of general internal logic resources in the FPGA to achieve, so the implementation of Altera FPGA embedded system is with great flexibility. As Nios becomes more and more successful, Altera company's SOPC concept has also been accepted by the majority of users.

Galaxian is a famous game that developed by Japanese company Namco in 1979, and is representative of the company's early classic game. Although the game has already been transplanted to the modern PC successfully, compared with the general structure of PC and ARM products, we use of FPGA architecture to develop, which can be programmed on both the system hardware and software which comes with greater flexibility and operability. What's more, FPGA also has a wealth of external resources, providing development with more diversity. Since the application software and hardware on the system are both programmable, hardware and software are well fit with each other, which can greatly improve the efficiency of running software code and the performance of processor, therefore this design is with high development value.

In this paper, we choose Altera's Nios II EDS as the software development platform, using DE2-115 study & development board to build a small hardware system, and then use the C and VHDL language to develop the corresponding application software. The system hardware include: DE2-115 development board, VGA monitor, LTM touch screen, 23-key keypad PS2 and audio device. The game can be controlled not only by the keyboard, but also through LTM touch screen directly, which makes the game more convenient to operate. In addition, we set up seven grades for the game to increase the game's executability and difficulty, whereas gamers have only three opportunities to challenge, if it fails, the game is over. PS2 keypad is used for decoding the input information of the control buttons to control the game, DE2-115 FPGA chip is the main programming chip, audio is used for playing music that stored on the SD card in order to enhance the game effect, VGA monitor is used to display the game screen that is connected to the DE2-115 board.

II. ARCHITECTURE

This system is based on Nios II processor, through the development and expansion of peripheral devices and taking advantage of the configured IP core to achieve a more intelligent control. By a close cooperation the Peripheral devices and central processor to achieve the desired results.

The game hardware system is dominated by VGA module, LTM touch screen module, Audio output module, PS2 keyboard module, general IO, data and instruction memory, the central processor and other modules.

A. Graphic display modules

Most computer and external display devices are connected via analog VGA interface, the computer generates image information digitally, then the graphics in the digital/analog converter is converted into R, G, B primary color signals and lines & field sync signal, they are sent to the display device through the cable.

Generally VGA display system consists of three parts: the control circuit, the display buffer area and the video Bios program. The control circuit mainly complete timing occurs, the display buffer data manipulation, the master clock selection and D/A conversion functions; Display buffer area provides display data cache space; video Bios as a control program solidified in the graphics card 's ROM. The VGA module control circuit is shown in Fig. 1.

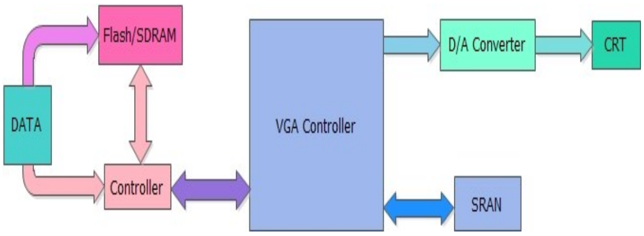


Fig. 1. VGA display module

B. LTM touch screen controller module

LTM touchscreen driver mainly relies to the LCD touch screen interrupt input pin position and data to determine coordinates of the touch action. The SPI bus driver judge interrupt pin level, and then locates the input pin by shifting the position coordinates and stores in the buffer register finally. That is transferred to the application layer of the software by the Avalon bus; the software reads the coordinates so as to control the game.

C. Audio output controller module

Audio processing uses the WM8371 chip, it first finds a music file, and then the music file is cut away the beginning and ending, leaving only the data part, and the data is converted to mif file which is written to the DE2-115 ROM. Audio controllers visits the ROM module to output a digital signal and the digital signal converts into an analog signal after pass an ADC converter, and finally arrives the audio output port.

D. PS2 keyboard controller module

PS2 keyboard is composed of two external IO and two clock pin and data pin which are used for connecting PS2 keyboard with DE2-115 board. Its internal clock signals has been kept on the keyboard data monitoring, once data has been detected arriving , then it immediately receive data through the shift register, then the data will be sent to the output buffer register for the software calls. The two IO pins respectively indicate that whether keys in the keyboard are pressed as well as whether the data has been read during data buffering period. It will help a lot in the software control and we can read the data obtained from PS2 keyboard to control the game results. The system structure is shown in Fig. 2.

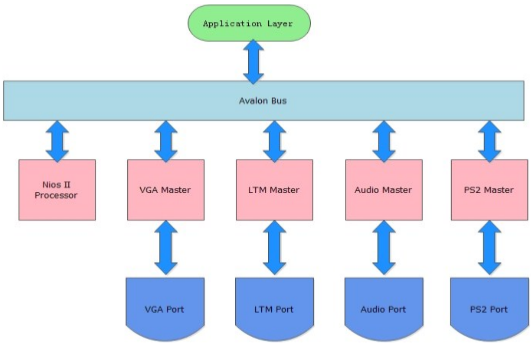


Fig. 2 The system structure

III. Hardware Design

The system is divided into hardware and software components. The hardware provides control interface and perform tasks operations for the peripherals. The hardware structure is shown in Fig.3.

We will give a detail introduction to them as following.

A. VGA reconfigurable IP core design

The reconfigurable IP core is that we can change some basic properties of the IP core to information in the IP core is conveyed by the Avalon bus, and then we can check the address that we have deployed. If the data is different, the configuration information in the IP core will change as well.

So we can use the software to configure some important parameters to control the operation of the IP module. Operate mode is shown in Fig. 4.

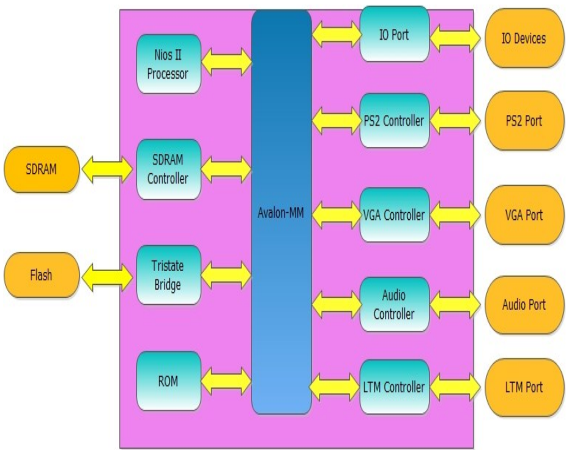


Fig. 3 Hardware block

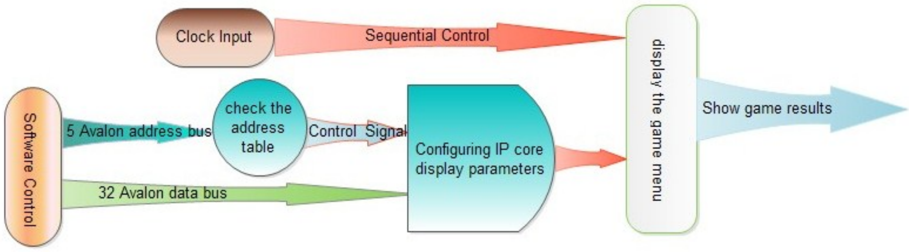


Fig. 4 Reconfigurable IP core operate mode

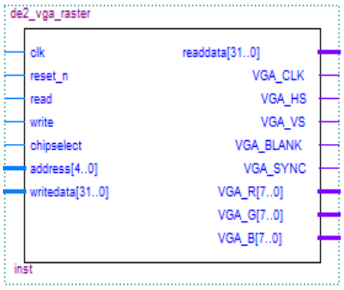
Table 1 shows the IP core address:

TABLE I

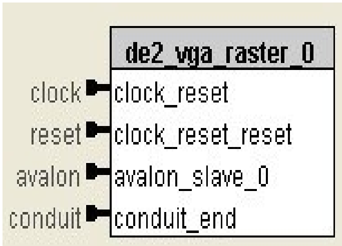
IP ADDRESS CONFIGURATION

address		**Writedata**			**utility**
H	S	Writedata(20-31)	Writedata(10-19)	Writedata(0-9)	
01100	48	Angle(25-31)+ Mode(22-24)+ Number(20-21)	FlyingV	FlyingH	Synchronization
01010	40	Bullet number	Bullet V	Bullet H	Enemy Bullet
01000	32	------	beeMatrixV	beeMatrixH	Formation
00111	28	------	planeV	planeH	plane
00110	24	------	Bullet V	Bullet H	Player Bullet
00101	20	One to five(21-25)	Alive		Enemy in Formation
00100	16	Control signal (1)	StartPicV		Start Screen
		Control signal (2)	Level（1-7）+player life (0-3)		Level & Player Life
		Control signal (3)			Clear Screen
		Control signal (4)	1(show) 0(hide)		Ready
		Control signal (5)	EndV	EndH	Game over
00011	12	plane explosion	Explosion V	Explosion H	plane explosion
00010	8	Flying explosion	Explosion V	Explosion H	Flying explosion
00001	4		High Score		High Score
00000	0		Current Score		Current Score

In this system, VGA and LTM IP core design use this idea. The software can transmit data via the Avalon bus to change the VGA control. Its IP core model is shown in Fig. 5.



(a)VGA IP core top-level design



(b) VGA IP core symbol

Fig. 5 VGA IP core design

IP core's Avalon interfaces directly connected to the Avalon bus. It provides address and I/O data. The conduit interfaces connected to the VGA external pin. So we can control the VGA display through the I/O.

B. LTM touch screen controller IP core design

We take the touch screen that provided by Terasic is TRDB-LTM 4.3 inch digit LCD touch panel. The aspect ratio is 15:9. It supports 24-bit parallel RGB interface and includes built-in contrast, brightness and gamma modulation module. It transits X / Y coordinates of the touch point into digital information through the ADC (AD7843). The structure is shown in Fig. 6.

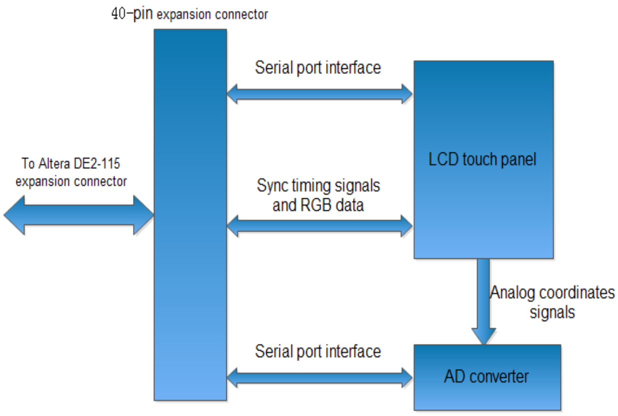


Fig. 6. LTM touch screen structure

LTM reconfigurable IP core design is the same with the VGA IP core design. There are some differences in the control timing between them. What's more, the LTM IP core has a driven management section for the touch screen. LTM includes three main modules: a serial interface, RGB data of the LCD display, SPI interface.

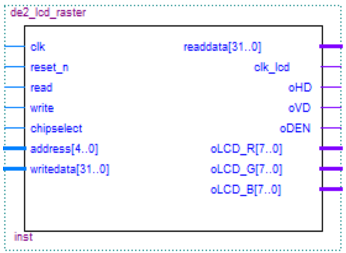
LTM display timing is shown in table 2. Horizontal timing and frame timing need to produce Sync, back porch, display interval, front porch.

TABLE II

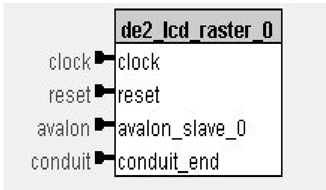
LTM DISPLAY TIMING

	Sync	back porch	Display interval	Front porch
H	0	216	800	40
V	0	35	480	10

The LTM's IP core model is shown in Fig. 7.



(a)LTM core top-level design



(b) LTM IP core symbol

Fig. 7 LIM IP core design

C. PS2 keyboard controller module

PS2 keyboard interface uses a bidirectional synchronous serial protocol that each send a pulse on the clock line , the data bus will send a bit data. The PS2 timing is shown in Fig. 8.

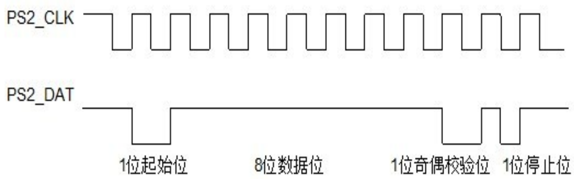
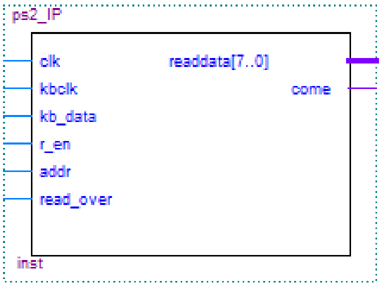
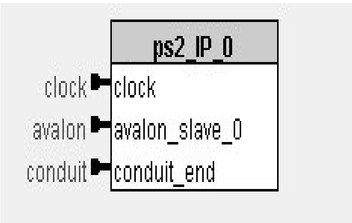


Fig. 8. PS2 Timing

The keyboard in this project is used to let the player control the space ship in the game. Though as an input device, it does not have much communication with other block in the FPGA architecture. With the SPOC builder, the data from keyboard can be visited from Avalon bus in the C code. Then, the software will send the corresponding new coordinates to the VGA raster and update the position of the space ship. Thus, the control of the game is realized. The PS2 keyboard IP core module is shown in Fig. 9.



(a)PS2 core top-level design



(b) PS2 core symbol

Fig. 9 PS2 IP core design

The kbclk and kb_data is used to accept the data that transmitted by the PS2 and then the data will be stored in the buffer register. Software read the data by visiting the register address. The come and read_over interface is a kind of response mechanism. When the keyboard generates a keystroke, the come port will tell the register that the data can be read. By this response mechanism, we can ensure the accuracy of reading data.

D. Audio module

The sound output in the game is implemented with WM8731 Audio CODEC (combining ADCs and DACs) provided on the DE2-115 board .However, in our project, we will not synthesis the sound but load the saved music file in directly in the audio module. The describing of the working process of the audio module is shown in Fig. 10.

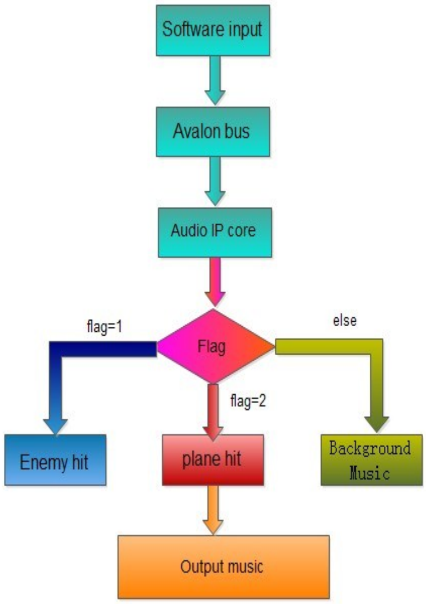
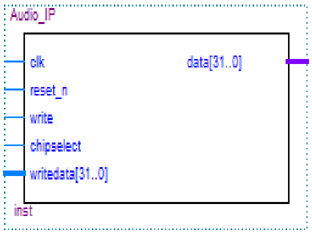


Fig. 10 Audio module working process

In this project, we implemented three kinds of music. One is the sound of the plane firing, one is the sound for explosion and the last one is for the enemy attacking. If there is a conflict to choose which sound to play, our plan is that always play the sound that happens last. This is to say, if during the enemy attacking period we fire a bullet, it will then play the sound of firing the bullet.

The Audio IP core module is shown in Fig. 11.



(a)Audio core top-level design

(b) Audio core symbol

Fig. 11 Audio IP core design

IV. Software Implement

A. Software architecture and algorithms

1) Galaxian game software flow chart

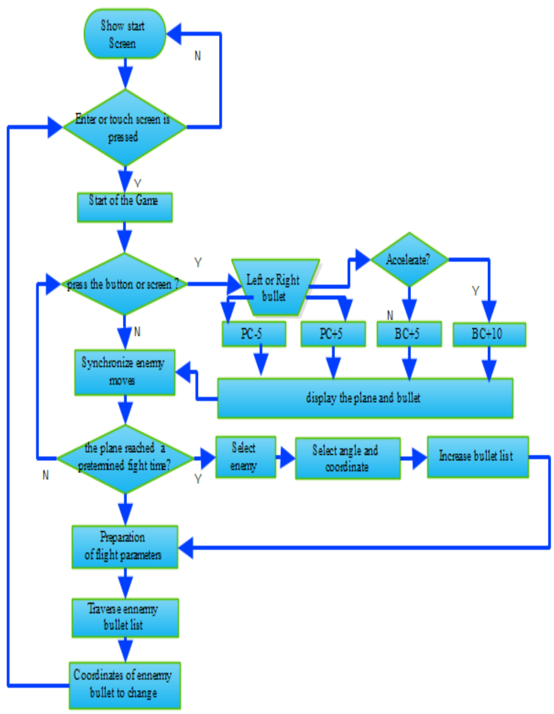


Fig. 12 Software float chat

2) Coordinate algorithm model

In order to save system resources, we don't assign position for each star – that would be 28 star vertical addresses and 28 horizontal addresses. Instead, we only assign position for the first star, and assign constant relative addresses for the rest of stars. In this way, the relative motions between stars remain zero, and every time we want to acquire all-star positions, we only need to calculate them based on the first star (say this "first star" has position of (base-coordinate-x, base-coordinate-y)).28 stars are distributed evenly in x-axis, and 4 phases of stars are alternatively distributed .To be more specific, four phases of stars' horizontal position are:

base-coordinate-x+88*i(i=0~6) (1)

base-coordinate-x+88*j+22(j=0~6) (2)

base-coordinate-x+88*m+44(m=0~6) (3)

base-coordinate-x+88*n+66(n=0~6) (4)

To make the dynamic effect obvious, we should ensure the distance between the galaxies Y-coordinates as far as possible. So we divided the vertical 480 pixels into 7 parts. For each phase, every star has a unique part.

Every star's vertical position can be expressed by base-Y-coordinate + vertical bias.

B. 360 degrees bees

The bee, which is flying down, can rotate 360 degrees. We only used 3 pictures to show 16 different pictures in our game. We use the idea of graphical mapping. First, we define the mapping area and the picture can be displayed in the mapping area. In the hardware, we also receive the signal about the angle of the flying bee. We maybe reversal or switch the x coordinate with y coordinate according to the signal of degree. While the bee matrix be connected with the order by the list. Then we can control the bee matrix. In order to ensure the symmetry line of flying bees, the random function is processed so that its random value can be uniformly appeared in the symmetric region.

Two-dimensional arrays implement the time management. First of all, the time parameters of the flying bee are stored in the array. According to the number of points at this time and the current number of bees, we can ascertain the delay time. The calculation model is as follows:

Time_index=waitTimeThreshold[level][flybe.num/6] (5)

The angle is also stored in an array. It stores the direction values that we have defined. The calculation model is as follows:

Angle_index=base-coordinate+16*flybee[i].column-currentline (6)

The path of the flying bee is managed by an array as well. We store the information into the array. So the change of the coordinates can determine the path change.

Fly_index=base-coordinate+flycount*flybee.angle; (7)

The 'bullet' is managed by a linked list. Bee array and aircraft's bullets are managed by the same kind of linked structure. First, we define an array of bullets; in each level the number of bullets need by the bees stored in an array. Then choose the certain array subscript according to the current level. In the process of flying bees, bee flight of steps once reach 20:00, it will add nodes to the current flying bees' bullets list, while the bee bullets only need to traverse the list.

V. EXPERIMENTAL RESULTS

The SOPC structure of our system is shown in Fig. 13. The system clock uses 50MHZ.

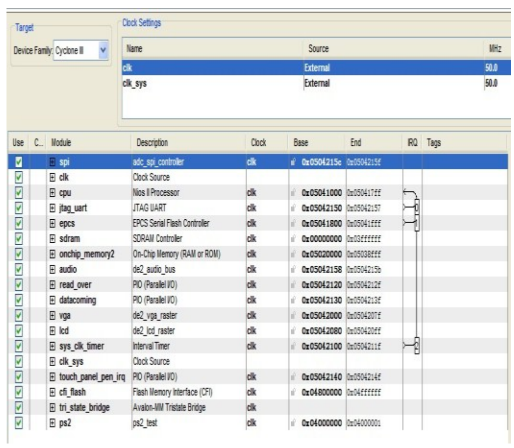


Fig. 13 SOPC builder interface

Then we will compilers the project in the Quartus II 10.1 About 29% of logic elements on the FPGA are used. The compilation result of our implementation is shown in Fig. 14.

Flow Summary	
Flow Status	Successful - Sun Jul 14 17:47:18 2013
Quartus II Version	10.1 Build 197 01/19/2011 SP 1 SJ Full Version
Revision Name	final
Top-level Entity Name	lab3
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	33,511 / 114,480 (29 %)
Total combinational functions	31,458 / 114,480 (27 %)
Dedicated logic registers	6,999 / 114,480 (6 %)
Total registers	7136
Total pins	189 / 529 (36 %)
Total virtual pins	0
Total memory bits	1,142,520 / 3,981,312 (29 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	2 / 4 (50 %)

Fig. 14 The report for the resource utility of our design based on DE2-115

The Quartus II compiled and generated the final .sof file; download the file to DE2-115 board, and then Nios II IDE designed software can be compiled to run the game. For offline use, we will solidify into DE2_115 software development board. Curing process is done by Nios II IDE Tool on the toolbar under the Flash Programmer to achieve. After curing, it can realize the power of hardware and software automatically loads the program, in order to achieve the game offline. Game runs effect diagram is following.

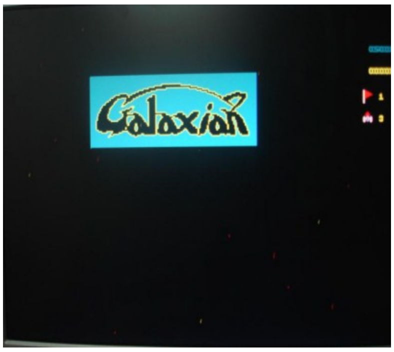


Fig. 14 Start interface

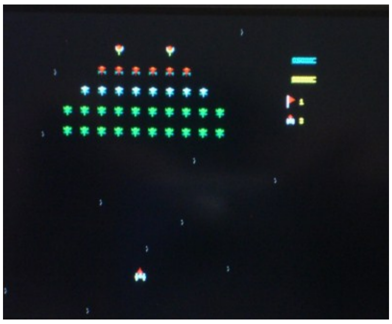


Fig. 15 Game running interface

Fig. 16 Gameover interface

VI. CONCLUSION

This is a classic and enjoyable game that calls up a lot of precious childhood memories. Since we have added a lot of modern elements and new ideas, with a lot of innovations in this project at the same time, which combines the widely used touch screen with computer games. As a result, this provides the players with the entertainment in dual visual and sensory. We have achieved the expected goal of the game, each module can work quite well. In the game the application of touch screen is a great innovation which makes the game controlling easier and better meet the requirements of the players. In recent years FPGA-based EDA technology is developing rapidly and its applications are increasingly being used on personal computers in the home, which is a great try and breakthrough of the game designing. It makes the way of using EDA tools to combine hardware and software with each other to be developed to a better direction; it is also a good driver of the promotion of SOPC technology. Therefore the design is of good development and promotion purposes. As the design of system is based on Nios II soft core, the system has a great flexibility that can design different games by changing the soft core, so that the system is of good compatibility, portability and application prospect.

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