Introduction of the Research Based on FPGA at NICS

Rong Luo

Nano Integrated Circuits and Systems Lab, Department of Electronic Engineering, Tsinghua University
Beijing, 100084, China
[1]luorong@tsinghua.edu.cn

Abstract — This document introduces the research work based on FPGA at Nano Integrated Circuits and Systems Lab, Department of Electronic Engineering, Tsinghua University.

Keywords — WSN Digital Baseband SOC, Two-dimensional Bar Code, Dynamic Time Warping Distance, Real Time Image Processing, FPGA

I. INTRODUCTION

The Nano Integrated Circuits and Systems Lab at the Department of Electronic Engineering, Tsinghua University, Beijing, China focus on the following research fields, Chips for Communications and Digital Media Processing, Electronic System Design Automation, Analog and Mixed-Signal Integrated Circuits Design, and Design of Radio-Frequency and Microwave Integrated Circuits.

In the field of Chips for Communications and Digital Media Process, research activities include ASIC design for wireless communication, digital broadcasting, and digital media applications.

A field-programmable gate array (FPGA) is a chip designed to be configured by a customer or a designer after manufacturing.[1] Hence, "field-programmable" is the biggest advantages, which can let the researcher update the functionality after shipping, partial re-configuration of a portion of their design. Moreover, with the ability of the low non-recurring engineering costs relative to an ASIC design, FPGAs offer advantages for many applications.

The structure of this paper is arranged as follows. Section II introduces the prototype system for our wireless sensor network digital baseband system-on-a-chip design based on DE2-70. Section III presents the implementation of an embedded two-dimensional bar code recognition system based on DE2. A subsequence similarity search algorithm based on Dynamic Time Warping (DTW) distance, is accelerated in Section IV. A hardware platform for a real time image processing system is built in Section V. Finally, the conclusions and acknowledgements are given.

II. BUILDING THE PROTOTYPE SYSTEM FOR WSN DIGITAL BASEBAND SOC DESIGN

Wireless Sensor Networks (WSNs) are widely used as information acquisition and processing platforms in many applications.

In order to design all digital WSN baseband SOC, a prototype based on DE2-70 is built to verify our design, as shown in Figure 1.[2]

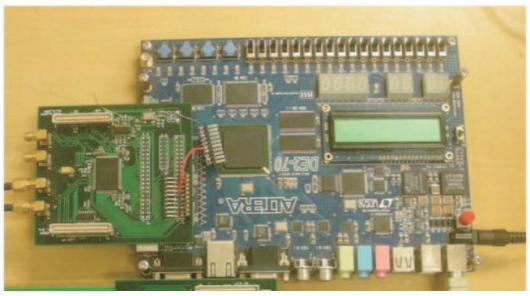

Figure 1. Prototype based on DE2-70[3] for WSN digital baseband SOC design

To meet the requirements of low complexity, low power and high flexibility, many algorithms are proposed, such as modulation, demodulation, spreading and synchronous, digital frequency converter, interpolation and decimation filter. According to the proposed algorithm, the architecture of our baseband circuit design is implemented in the prototype.

As shown in Figure 2, the MCU core 8051 consumes 3427 LUTs, while the baseband circuits consume 3282 LUTs. The resource of DE2-70 is more than enough for our design.

Entity	Logic Cells	Dedicated Logic Reg.	Memory Bits	M4Ks	Pins	LUT-Only LCs	Register-Only LCs
Cyclone II: EP2C70F896C6							
wcu_cov	13830 (8)	7078 (5)	133632	36	142	6752 (1)	1084 (0)
SBGT_LUT_2:SBG7	14 (0)	0 (0)	0	0	0	14 (0)	0 (0)
SBGT_LUT_2:SBG72	14 (0)	0 (0)	0	0	0	14 (0)	0 (0)
SBGT_LUT_2:SBG73	14 (0)	0 (0)	0	0	0	14 (0)	0 (0)
mc8051_top:b2v_inst1	3955 (0)	520 (0)	132096	33	0	3427 (0)	24 (0)
conv2:b2v_inst3	0	0	0	0	0	0	0
spi_baseband:b2v_inst5	9827 (0)	6545 (0)	1536	3	0	3282 (0)	1060 (0)
flash_cov:b2v_inst8	8 (8)	8 (8)	0	0	0	0 (0)	0 (0)

Figure 2. Resource Consumption of Cyclone II

III. IMPLEMENTING AN EMBEDDED TWO-DIMENSIONAL BAR CODE RECOGNITION SYSTEM BASED ON FPGA

A two-dimensional bar code is a symbol in the plane, which has particular shape both in its horizontal and vertical direction. Therefore, it has the ability of carrying more information in smaller area with higher error tolerance as well as better scalability compared to a one-dimensional bar code.[4]

As an open standard, PDF417 code is adopted to design an embedded two-dimensional bar code recognizing system based on FPGA using the NIOS II processor[5], as shown in Figure 3.

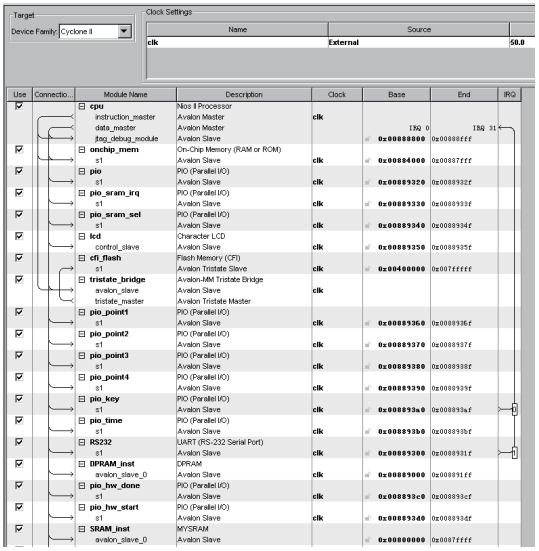

Figure 3. The whole configuration for NIOS II processor

Figure 4 show the report for the resource utility of our design based on DE2. The software-based system can finish the recognition in 28ms with 90% accuracy, given a 320 * 240 two-dimensional bar code image.

Flow Status	Successful - Thu Jun 02 19:47:02 2011
Quartus II Version	7.2 Build 151 09/26/2007 SJ Full Version
Revision Name	DE2_TV
Top-level Entity Name	DE2_TV
Family	Cyclone II
Device	EP2C35F672C8
Timing Models	Final
Met timing requirements	No
Total logic elements	28,631 / 33,216 (86 %)
Total combinational functions	25,378 / 33,216 (76 %)
Dedicated logic registers	14,078 / 33,216 (42 %)
Total registers	14127
Total pins	430 / 475 (91 %)
Total virtual pins	0
Total memory bits	242,256 / 483,840 (50 %)
Embedded Multiplier 9-bit elements	70 / 70 (100 %)
Total PLLs	1 / 4 (25 %)

Figure 4. The report for the resource utility of our design based on DE2[6]

IV. ACCELERATING SUBSEQUENCE SIMILARITY SEARCH BASED ON DYNAMIC TIME WARPING DISTANCE WITH FPGA

Subsequence search, especially subsequence similarity search, is one of the most important subroutines in time series data mining algorithms, and Dynamic Time Warping (DTW) distance is best. Although many software speedup techniques, including early abandoning strategies, lower bound, indexing, computation-reuse, DTW still cost about 80% of the total time for most applications. Moreover, DTW is hard to use parallel hardware to be accelerated because it is 2-Dimension sequential dynamic search with quite high data dependency.

A novel framework for FPGA based subsequence similarity search and a novel PE-ring structure for DTW calculation are proposed.[7] Figure 5 illustrates the framework.

The framework utilizes the data reusability of continuous DTW calculations to reduce the bandwidth and exploit the coarse-grain parallelism, and guarantees the accuracy with two-phase precision reduction. The PE-ring supports on-line updating patterns of various lengths, and utilizes the hard-wired synchronization of FPGA to realize the fine-grained parallelism, which can only be exploited by FPGAs.

Our system is implemented on TERASIC Company's Altera DE4 Board with a Stratix IV GX EP4SGX530 FPGAs.[8]

The resource cost of our system is shown as Figure 6.

Combinational ALUTs	362,568/424,960	(85%)
Dedicated logic registers	230,160/424,960	(54%)
Memory bits	1,902,512/21,233,664	(9%)

Figure 6. The report for the resource cost of our system based on DE4

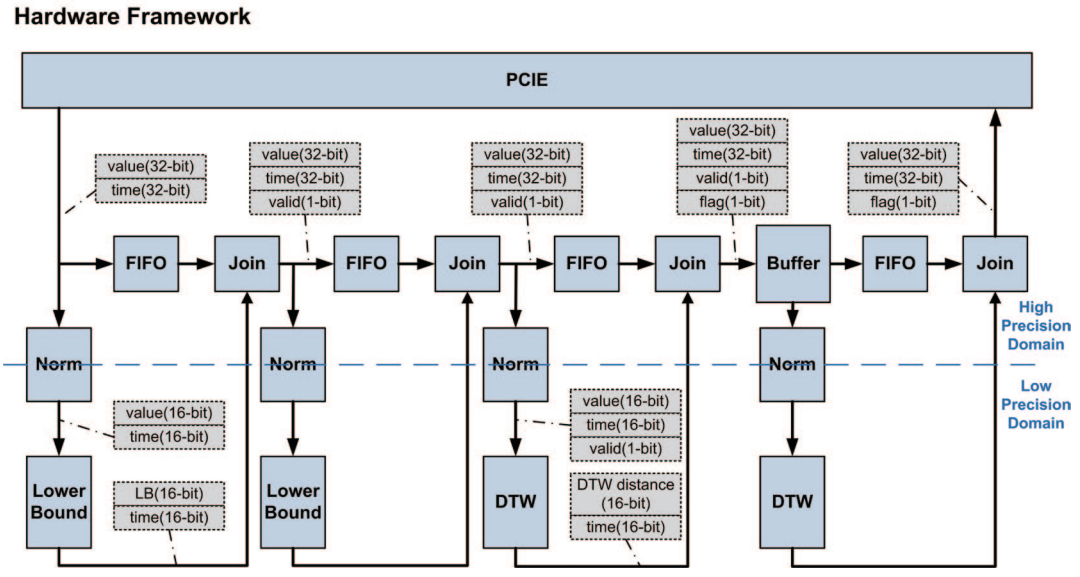

Figure 5. Hardware framework of the DTW system

The experimental results show that this work achieves one to four orders of magnitude speedup compared to the best software implementation in different datasets, three orders of magnitude speedup compared to the current GPU implementations, and two orders of magnitude speedup compared to the current FPGA implementation.

V. CONSTRUCTING A DETECTION AND 3D MEASUREMENT FPGA BASED SYSTEM FOR A REAL TIME IMAGE PROCESSING

Electronic Road Pricing (ERP) system is widely used in the world. The first large scale free flow road pricing system has been successfully in operation in Singapore since April 1998, in which an enforcement system (vehicle detection and license plate recognition) has achieved the performance of success rate of license plate recognition as 96% in 1.5 million pieces of vehicle units. However, the performance is based on lots of high quality of equipments with high cost, such as in-vehicle-units for every vehicle, complex gantries with many sensors, high luminance lighting, and high resolution cameras. As a result, reducing system cost is the most important issue for expanding sales for other countries. [9]

In some markets, the use of only video cameras for the enforcement system to identify the vehicles might be a cost reduction option since complex gantries would be removed. A simple enforcement system with video cameras offers high performance solutions with very low initial investment. Stereo cameras are needed to assure the tolling accuracy. Due to the fact that cameras, especially stereo ones, will provide really large real-time video for the tolling system to detect and classify the vehicles, a real-time and high throughput image processor is very necessary.

FPGA has millions of LEs (Logic Elements) processing at the same time in a parallel way and this feature can achieve high parallelism and throughput which fit for the real-time vehicle detection and classification algorithms from the video. However, in order to achieve high performance and low cost using FPGA, the key problem is how to reasonably analyze the computation cost and computation load allocation of vehicle detection and classification algorithms. Thus, we design the FPGA based detection and tracking processing system.

Based on simulation by ModelSim SE 6.5 and synthesis by Quartus II 10.0, the hardware implementation on Altera Stratix IV FPGA can reach 125MHz. It could achieve about 43 fps for video of 1392*1040 resolution with a large disparity range of 256, and 400 fps for a video of 640*480 resolution with a disparity range of 128. The detection and tracking part only gives the tracked area, so the image for these modules is resized to 320*256. We keep the 1392*1040 resolution for stereo matching in order to achieve more accurate size extraction.

The software results are tested on an i7 930 2.8GHz CPU based on OpenCV library. The results as shown in Table I indicates that our FPGA implementation of the system has 71.38 times speedup than software, and 63.91 times speedup for stereo matching.

TABLE I
SW AND HW RESULTS FOR ONE 1392*1040 IMAGE

Module	Software(ms)	Hardware(ms)	Speedup
Detection	161.42	2.42	66.70
Stereo Matching	1380.40	21.60	63.91
Total	1541.82	21.60	71.38

CONCLUSIONS

In summary, with the outstanding abilities of FPGA, much research work is done based on FPGA at NICS lab.

This paper introduces four projects. The prototype system for our wireless sensor network digital baseband system-on-a-chip design based on DE2-70 helps us to verify our proposed circuits and algorithms. The implementation of an embedded two-dimensional bar code recognition system based on DE2 shows that the proposed design can finish the recognition in 28ms with 90% accuracy, given a 320 * 240 two-dimensional bar code image. A subsequence similarity search algorithm based on Dynamic Time Warping (DTW) distance, is accelerated in DE4. Compared with other software and hardware methods, it can achieve at least two orders of magnitude speedup. A hardware platform for a real time image processing system is built based on DE4, and experimental results demonstrate that our FPGA implementation of the system has 71.38 times speedup than software, and 63.91 times speedup for stereo matching.

ACKNOWLEDGMENT

Many thanks to Altera Corp. for supplying excellent FPGA chips, and TERASIC Company for their powerful DE series boards.

Many thanks to National Science and Technology Major Project of the Ministry of Science and Technology of China, National Natural Science Foundation of China, Microsoft and Mitsubishi Heavy Industries for their financial support.

Many thanks to prof. Huazhong Yang, Yu Wang and Yongpan Liu for their contributions to the research work at NICS.

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