FPGA Implementation of an Efficient Two-dimensional Wavelet Decomposing Algorithm

[#]Chuanyu Zhang, [*]Chunling Yang, [#]Zhenpeng Zuo

School of Electrical Engineering, Harbin Institute of Technology
Harbin, China
[1]zcypolaris@163.com, [2]zuozhenpeng@163.com, [3]yangcl1@hit.edu.cn

Abstract — As the preferred method for the multi-resolution analysis of the image, discrete wavelet transform has gained more and more attentions. In this paper, a new VLSI architecture is designed to finish two-dimensional all at once. Through further derivation of the transform formulas, line based method is improved and the circuit structure is simplified. The FPGA implementation has been achieved on an Altera Cyclone II EP2C35F672C6. Results show that this improvement results in a considerable performance gain while reducing the consumption of on chip memory space and shortening output latency significantly. Under pure calculation logic, processing speed reaches 157.78MHz.

Keywords — wavelet transform, image processing, FPGA, VLSI, SOPC

I. INTRODUCTION

DWT is the preferred mathematic tool when it comes to observing and processing digital images. The lifting scheme is a fast implementation of wavelet transform, the procedure of filtering can be decomposed to several steps. Thus the amount of computation and memory space are reduced significantly. Also, it is quite suitable for in-place calculation and hardware implementation.

At present, there are two kinds of widely used VLSI architectures to realize 2-D lifting wavelet transform: the line based ones and the frame based ones. As research processes, new VLSI architectures come into being continuously. Although the performance of the circuits advanced gradually, low complexity still conflicts with low cost of memory space. In this paper, we put forward a new VLSI architecture for 2-D lifting wavelet transform which simplifies the circuit complexity and saves memory space greatly. That is how the overall performance of the circuit is improved.

II. WAVELET LIFTING ALGORITHM

A. Lifting Wavelet Transform

To achieve wavelet transform through the lifting scheme, there are three steps: Split, Prediction and Update. In the discrete situation, input data set p_k is split into two subsets to separate the even samples from the odd ones. After lifting scheme processing, the detailed coefficients s_k and the wavelet coefficients d_k are generated. Take Le Gall 5/3 wavelet for instance, the procedure of 1-D integer wavelet decomposition could be described by figure 1.

The lifting 5/3 wavelet algorithm is described as follows:

$$d_k = p_{2k+1} - (p_{2k} + p_{2k+2})/2 \quad (1)$$

$$s_k = p_{2k} + (d_k + d_{k-1} + 2)/4 \quad (2)$$

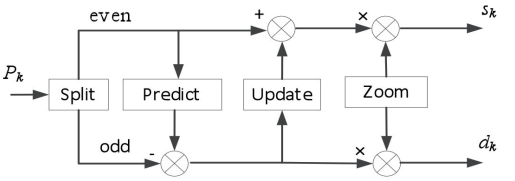

Figure 1. Split, predict and update phases of the lifting based DWT

Where p_k is original pixel data set, d_k is high frequency of transform result and s_k is the low frequency one.

The procedure of accomplishing 2-D transform is as follows: with line transform original image is divided into two sub-bands, and with a column transform they are divided into four sub-bands. Each sub-band is 1/4 size of the initial image. We can realize the next level wavelet transform as long as we do transform to LL sub-band in the same way. Figure 2 shows the procedure of three level wavelet transform.

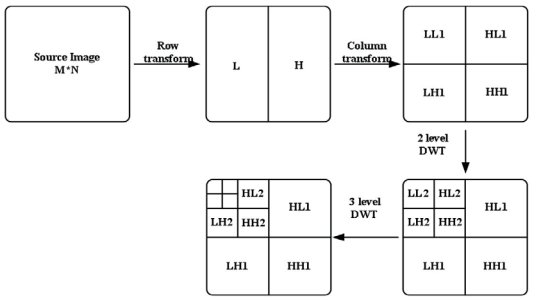

Figure 2. Theory of two-level DWT

For the reason that transform is proceeded in the column direction, he result of row transform must be input column by column. Large amount of middle data must be stored. That is why the cost of hardware is immense and the speed of data processing is limited.

B. Further Derivation for Two Dimensional Transform

We substitute expression (1) into expression (2) to get a 2-D transform VLSI architecture with a better performance:

$$s_k = (-p_{2k-2} + 2p_{2k-1} + 6p_{2k} + 2p_{2k+1} - p_{2k+2} + 4)/8 \quad (3)$$

In order to conduct 2-D wavelet image, further derivations of the transform formulas are necessary. The image pixels at row i and column j will be denoted as $p_{i,j}$. After getting the results of line transform, apply the formula to vertical direction to proceed column transform. Take the results of twice of the low filtering for instance, the correlation is:

$$\begin{aligned} p_{i,j}^{LL} = (&p_{2i-2,2j-2} - 2p_{2i-2,2j-1} - 6p_{2i-2,2j} - 2p_{2i-2,2j+1} + p_{2i-2,2j+2} \\ &-2p_{2i-1,2j-2} + 4p_{2i-1,2j-1} + 12p_{2i-1,2j} + 4p_{2i-1,2j+1} - 2p_{2i-1,2j+2} \\ &-6p_{2i,2j-2} + 12p_{2i,2j-1} + 36p_{2i,2j} + 12p_{2i,2j+1} - 6p_{2i,2j+2} \\ &-2p_{2i+1,2j-2} + 4p_{2i+1,2j-1} + 12p_{2i+1,2j} + 4p_{2i+1,2j+1} - 2p_{2i+1,2j+2} \\ &+p_{2i+2,2j-2} - 2p_{2i+2,2j-1} - 6p_{2i+2,2j} - 2p_{2i+2,2j+1} + p_{2i+2,2j+2})/64 + 1/2 \end{aligned} \quad (5)$$

Take the coefficients into determinant shown in figure 3(1).

Similarly, for the sake of getting the horizontal high frequency-vertical low frequency output (HL), the horizontal low frequency-vertical high frequency output (LH) and the horizontal high frequency-vertical high frequency output (HH), we can apply (1), (3) into 2-D transform in the same way. Determinants are shown as follows:

$$\begin{vmatrix} 1 & -2 & -6 & -2 & 1 \\ -2 & 4 & 12 & 4 & -2 \\ -6 & 12 & 36 & 12 & -6 \\ -2 & 4 & 12 & 4 & -2 \\ 1 & -2 & -6 & -2 & 1 \end{vmatrix}$$ (1)LL

$$\begin{vmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & -2 & -6 & -2 & 1 \\ -2 & 4 & 12 & 4 & -2 \\ 1 & -2 & -6 & -2 & 1 \\ 0 & 0 & 0 & 0 & 0 \end{vmatrix}$$ (2)HL

$$\begin{vmatrix} 0 & 1 & -2 & 1 & 0 \\ 0 & -2 & 4 & -2 & 0 \\ 0 & -6 & 12 & -6 & 0 \\ 0 & -2 & 4 & -2 & 0 \\ 0 & 1 & -2 & 1 & 0 \end{vmatrix}$$ (3)LH

$$\begin{vmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & -2 & 1 & 0 \\ 0 & -2 & 4 & -2 & 0 \\ 0 & 1 & -2 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{vmatrix}$$ (4)HH

Figure 3. Determinants of filter coefficients

III. DESIGN OF ARCHITECTURE

A. System Architecture

For 2-D DWT, we put forward an implementation of the lifting wavelet transform based on the formulas deduced from figure 3. System structure diagram is given in figure 4.Initial image data are read out from external memory, after edge expanding in the expand unit, they are sent into buffer units and then sent into the 2-D DWT processing module, creating four sub-band sets of data. After sampling, the results are sent to the VGA monitor to present. Each part of the system work under a certain timing sequence generated by the control modules of the system.

B. Design of Two-dimensional transformation module

In the process of 2-D wavelet decomposition of a digital image, the 2-D transform processor is the significant unit and influents the timing design of the system and its performance.

From the determinants given in figure 3, we can draw the conclusion that the process of the 2-D transform is in fact weighted summation from a 5×5 sampling window. Calculations in this process are mainly multiplications and additions. For example, equation (4) corresponds to Determinants

$$\begin{vmatrix} p_{2i-2,2j-2} & p_{2i-2,2j-1} & p_{2i-2,2j} & p_{2i-2,2j+1} & p_{2i-2,2j+2} \\ p_{2i-1,2j-2} & p_{2i-1,2j-1} & p_{2i-1,2j} & p_{2i-1,2j+1} & p_{2i-1,2j+2} \\ p_{2i,2j-2} & p_{2i,2j-1} & p_{2i,2j} & p_{2i,2j+1} & p_{2i,2j+2} \\ p_{2i+1,2j-2} & p_{2i+1,2j-1} & p_{2i+1,2j} & p_{2i+1,2j+1} & p_{2i+1,2j+2} \\ p_{2i+2,2j-2} & p_{2i+2,2j-1} & p_{2i+2,2j} & p_{2i+2,2j+1} & p_{2i+2,2j+2} \end{vmatrix}$$

And figure 3(1).

Set a certain column in the sampling window as vector $(p_1, p_2, p_3, p_4, p_5)$, Each clock period, column vectors in the sampling window will move one position to the right, and the most left a list of data will be updated. Set a certain column in determinants in figure 3 as $A=(a_1, a_2, a_3, a_4, a_5)$, the basic calculation will be $(p_1, p_2, p_3, p_4, p_5) \times (a_1, a_2, a_3, a_4, a_5)^T$.

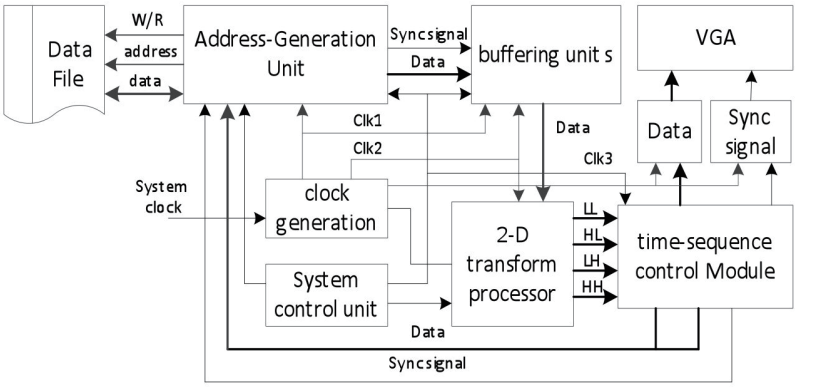

Figure 4. System architecture

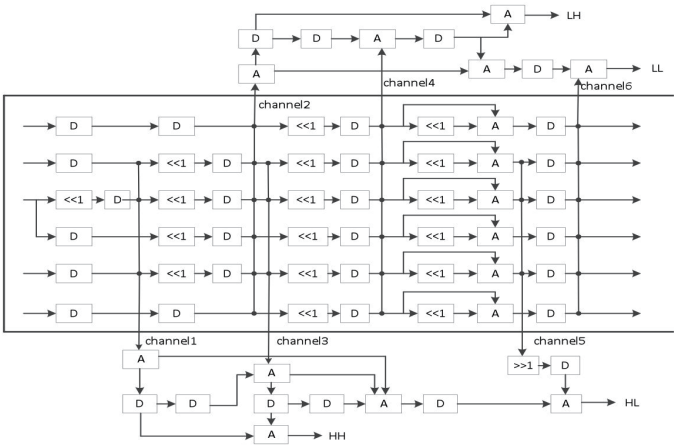

Figure 5. Inner structure of 2-D DWT processor

We can conclude from figure 4 that A has 6 different values: A_1=(1, -2, -6, -2, 1)^T, A_2=(-2, 4, 12, 4, -2)^T, A_3=(-6, 12, 36, 12 ,-6)^T, A_4=(0, 1, -2, 1, 0)^T, A_5=(0, -2, 4, -2, 0)^T, A_6=(0, -6, 12, -6, 0)^T. And A_3= $3A_2$ = -$6A_2$, A_6 = $3A_5$ = -$6A_4$.

On the basis of the determinants in figure 3, the processor's definite structure denotes in figure 5.

Parameter relationships between channels and vectors are:

TABLE I. PARAMETER RELATIONSHIPS BETWEEN CHANNELS AND VECTORS

channel	Vector A
channel 1	A_4 = (0, 1, -2, 1, 0)^T
channel 2	A_1 = (1, -2, -6, -2, 1)^T
channel 3	A_5 = (0, -2, 4, -2, 0)^T
channel 4	A_2 = (-2, 4, 12, 4, -2)^T
channel 5	A_6 = (0, -6, 12, -6, 0)^T
channel 6	A_3 = (-6, 12, 36, 12, -6)^T

This structure includes 15 adders, 18 shifters and 34 delay-units, no more extra multiplying units are needed. It can be estimated that if this 1-D 5/3 wavelet transform architecture is achieved on an FPGA chip, the number of logic units occupied will be 40A (A stands for bit width of the initial data)

$$N_{clk} = L_d + W = L_d + \frac{2}{3}N^2(1-\frac{1}{4^L}) \qquad (5)$$

Where L_d stands for the delay between line transform and column transform, in our design L_d=*0*, in other words, there are no middle data generates, so plenty of memory space is saved and delay between line transform and column transform is eliminated. What's more, although the number of data read operation of the external memory increases by a little, the working time of processor decreases sharply. That is the reason why the system consumption reduces obviously.

IV. RESULTS AND ANALYSIS

In order to test the performance of the architecture we design and observe the result intuitively, we realize simulation of the processor module with MODELSIM 6.5, as figure 6 shows.

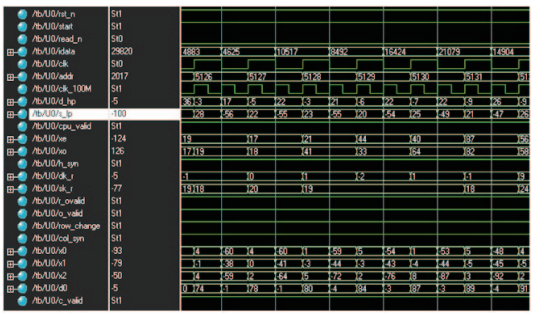

Figure 6. The simulation of 2-D DWT

We compare the 2-D DWT architecture we designed with others in terms of on-chip memory space, control difficulty and hardware complexity in Table II.

TABLE II. PERFORMANCE COMPARISON OF 5/3 2-D DWT ARCHITECTURES

Architecture	Lit. [3]	Lit. [4]	Lit. [5]	Lit. [6]	Our Design
Shifter	16	4	4	4	18
Adders	16	8	8	8	15
Memory on-chip	$5N$	N^2+4N	$6N$	$5N$	5
Memory off-chip	$N^2/4$	0	0	$N^2/4$	0
Computing time	$2N^2(1-4L)/3$	$2N^2(1-4L)/3$	N^2	$2N^2(1-4L)/3$	$2N^2(1-4L)/3$
Output latency	$2N$	$2N$	$2N$	$5N$	0
Utilization rate	100%	100%	50%	100%	50%
Complexity	Medium	Medium	Complex	Simple	Simple

CONCLUSIONS

This paper presents a new VLSI architecture for the lifting wavelet transform, Le Gall 5/3 wavelet taken as example. As a development of line base method, this architecture is advisable for its simple structure, high flexibility and low requirement of memory. Under pure calculation logic, processing speed reaches 157.88MHz.

Function and performance testing are conducted on an FPGA chip Cyclone II EP2C35F672C6, and we come to the conclusion that the intended targets have been achieved.

REFERENCES

[1]. Gonzalez, Digital Image Processing [M]. Beijing: Electronic Industry Press, 2005.9:179.

[2]. W. Sweldens, "The Lifting Scheme: A Chustom-Design of Biothogonal Wavelets," Data Compression Conference, 1996, 3(2): pp. 186-200.

[3]. Chrysafis C, Ortega A. Line Based, Reduced Memory, Wavelet Image Comperssion[C]. IEEE Trans. On Image Processing, 1998:398—407

[4]. Andra K; Chakrabarti C; Acharya T, A VLSI architecture for lifting-based forward and inverse wavelet transform[J]. IEEE Trans. Signal Process., 2002, 50(4): 966–977

[5]. Liao H; Mandal M K; Cockburn B F, Efficient architectures for 1-D and 2-D lifting-based wavelet transforms[J]. IEEE Trans. Signal Process., 2004, 52(5): 1315–1326

[6]. Barua S; Carletta J E; Kotteri K A, An efficient architecture for lifting-based two-dimensional discrete wavelet transform, Integr[J]. VLSI J., 2005, 38(3): 341–352

[7]. Maamoun M; Bradai R. Low Cost VLSI Discrete Wavelet Transform and FIR Filters Architectures for Very High-Speed Signal and Image Processing[C]. IEEE 9th International Conference on Cybernetic Intelligent Systems (CIS), 2010:1-6

[8]. Chao Sun. Hardware realization of the image compression algorithm Based on the wavelet transform [D]. Harbin: Harbin Institute of Technology, 2009: 3-5

[9]. TANG Y; CAO J; LIU B, FPGA Design of Wavelet Transform in Spatial Aircraft Image Compression [J]. Computer Science, 2010, 37(9):261-263

[10]. Tewari G; Sardar S; Babu K A , High-Speed & Memory Efficient 2-D DWT on Xilinx Spartan3A DSP using scalable Polyphase Structure with DA for JPEG2000 Standard[C]. International Conference on Electronics Computer Technology (ICECT) , 2011,1: 138 - 142