Implementing Full HD Video Splitting on Terasic DE3 FPGA Platform

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Abstract — This document introduces the design of HDMI Full HD 1080p splitting processor techniques in detail. It also describes how to design the proper DDR2 Multi-Port Controller to prevent the side effects of image processing like flickering and tearing. In addition to this, it shows the efficient DDR2 Multi-Port Controller to get the best performance, where the DDR2 can operate easily at 200 Hz with a 148.5 MHz Full HD input source, and hence there is no limit number of screen splitting.

Keywords — video split, DDR2 controller, Multi-Port memory controller, ping-pong buffer, TV wall

I. INTRODUCTION

As televisions are entering into the age of High Definition Television generation, HDTV can be separated into 720p, 1080i, and 1080p under the Rec.709 (ITU-R Recommendation BT.709)[1] protocol, where "i" stands for interlaced scanning and "p" stands for progressive scanning. Under a frequency of 60 Hz, a 1080i HDTV can display 30 complete frames a second, and 1080p can display 60 complete frames per second. Hence, 1080p is the most stable and smooth solution.

Under Full HD resolutions (1920 x 1080), the HDMI connector is an integral part of the interface. Under 720p transmission, 1.485 Gb/s is needed to support uncompressed video and audio content. With HDMI 1.0[2], 24-bit video can transfer at a speed of 165 megapixels per second, with the bandwidth reaching up to 4 Gb/s. This not only meets the requirements for displaying 1080p, it also supports 192 kHz sampling, which is able to transmit an 8-channel 24-bit LPCM audio signal as well.

Under HDMI 1.3[3], transfer speeds were increased from the original 4.96 Gb/s (165 Mpixels) to 10.2 Gb/s (340 Mpixels), and color depth was increased from 24-bit sRGB or YcbCr to 30-bit, 36-bit, and 48-bit xvYCC, sRGB, or YCbCr, which results in an output capacity of more than 100 million colors. With the recent development of the HDMI 1.4[4] standard, in addition to increasing the maximum resolution and expanding support for color spaces, 3D formats and even more features were added.

Under the current progress of HDTV and HDMI specifications, simple image splitting has become quite a challenge on hardware design. In order to split images to reach Full HD standards, video processing core design is the focal point. This paper presents the design methodology for HDMI Full HD1080p video splitting, implemented on a DE3 FPGA platform[5] in particular.

II. SYSTEM ARCHITECTURE

The basic HDMI Full HD 1080p block diagram for video processing core design is shown in Figure 1.

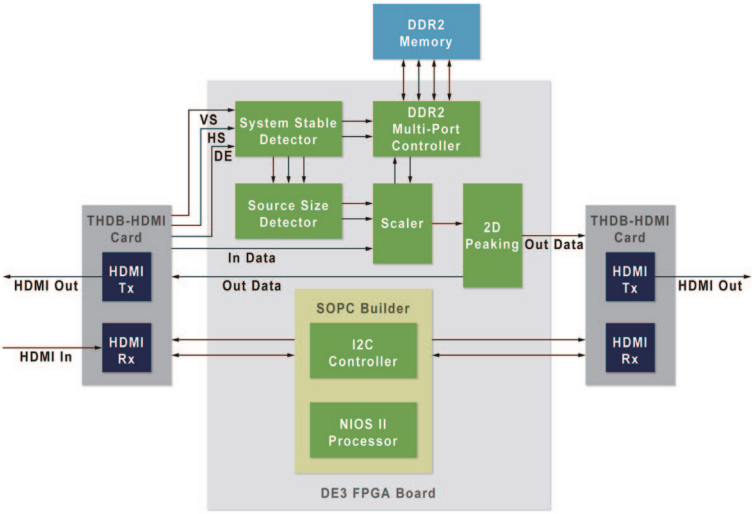

Figure 1. HDMI Full HD 1080p split-screen block diagram

The system receives an HDMI Full HD input, which after FPGA processing, is scaled vertically or horizontally according to the LCD screen. The image is then spanned across two (or four) 1920 x 1080 LCD screens. Figure 2 shows the actual setup of the DE3 FPGA hardware platform along with an HDMI daughter card for input/output, which meets the requirements of HDMI 1.4a.

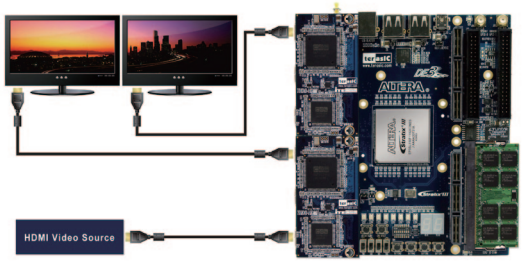

Figure 2. HDMI input/output using DE3 FPGA platform and daughter card under HDMI1.4a

The system is composed of three portions:

- HDMI input/output settings controller
- HDMI control signal generator
- HDMI video streaming processor

III. HDMI INPUT/OUTPUT SETTINGS CONTROLLER

For the first portion, in HDMI input/output settings, the controller core is established via the SOPC Builder in Figure 1. It is built with a combination of the Nios II Processor and I2C Controller, which are in charge of setting and controlling HDMI input/output.

IV. HDMI CONTROL SIGNAL GENERATOR

The second portion is the HDMI control signal generator, which is composed of the System Stable Detector, Source Size Detector, and DDR2 Multi-Port Controller in Figure 1.

A. System Stable Detector

The System Stable Detector is in charge of automatically detecting switching between different resolution sources, so that the whole system can reset to match.

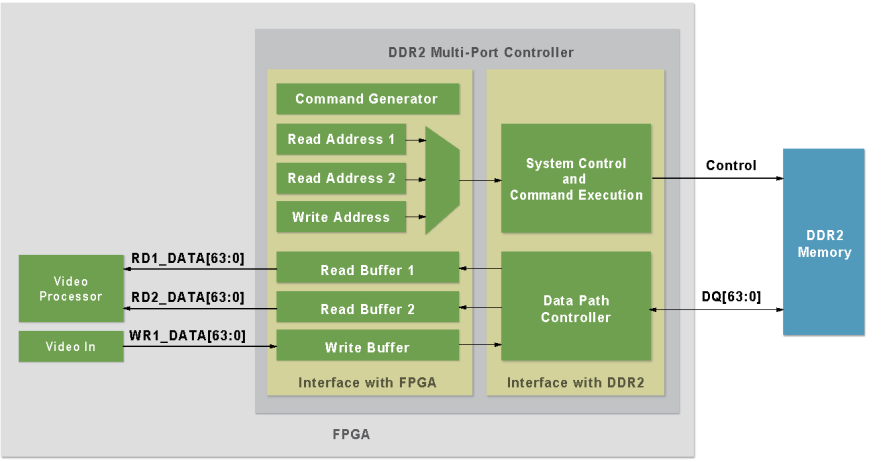

Figure 3. DDR2 Multi-Port Controller block diagram

B. Source Size Detector

The Source Size Detector is responsible for setting the proper scaling factor, frame size, and start position of display according to the ratio of the front-end source and back-end display.

C. DDR2 Multi-Port Controller

The DDR2 Multi-Port Controller is responsible for controlling the frame buffer access as the vertical-splitting mode. The DDR2 memory is set up as ping-pong buffer structure (Figure 4 is an example of vertical-splitting one image into two), utilizing two identical frame buffers. One frame buffer is written, and the other frame buffer is read, which prevents flicker and tearing.

If the screen is vertical split from one frame to two, the DDR2 Multi-Port must be set up as one write port and two read ports. The basic block diagram is shown in Figure 3.

During the writing stage, two starting positions must be identified, one for the top half of the image, and the other for the bottom half of the image, simplifying the read portion of the DDR2 controller architecture. In the design, the timings for the two read ports are equally allocated. As can be seen in Figure 4, only one read port is operation when one line is written, i.e. when the first line is written, only the first line of the top half buffer is read, and when the second line is written, only the first line of the bottom half is read, and so on.

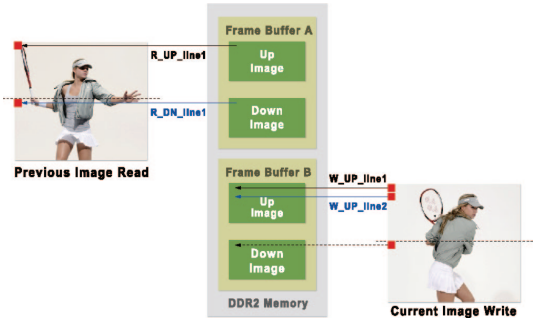

Figure 4. The DDR2 memory forms a ping-pong buffer architecture on the DE3 platform-vertical splitting

As such, the DDR2 bandwidth is allocated for the best performance, where the DDR2 can operate easily at 200 Hz with a 148.5 MHz Full HD input source, and hence there is no limit number of vertical splitting.

V. HDMI VIDEO STREAMING PROCESSOR

The third portion of the HDMI video streaming processor is made up of the Scaler and 2D Peaking unit in Figure 1.

A. Scaler

The Scaler is responsible for adjusting the input video source according to the predetermined-splitting number, either by linear or non-linear scaling up. During interpolation, the more reference points there are, the better quality of resulting image forms. It's better to at least use bi-cubic[6] interpolation. If edge-adaptive can also be considered, the high frequency images will be much clearer.

B. 2D Peaking

The 2D peaking is responsible for increasing the sharpness of the video, as after scale processing, edges appear blurry. It's important to note that if scaling is not performed properly, artifacts such as halos and jagged patterns may appear after 2D peaking operation.

CONCLUSION

The experimental platform is shown in Figure 2, with the DE3 FPGA development kit handling all the functions of receiving and transmitting HDMI. The Sony PlayStation 3 is the input HDMI source, generating a 1920 x 1080 Full HD progressive signal. The FPGA takes the front-end source and partitions it into two images, where it displays them on two separate HDMI monitors. Utilizing the Altera Stratix III 340 kit, with 340,000 logic elements, the experimental platform ran at 148.5 MHz, with the on-board DDR2 running at 200 MHz.

With the above mentioned design methodology, multiple frames (2x2, 2x3, 3x3, 4x4, etc.) can be formed with Full HD. Taking advantage of the re-stackable and modifiable nature of the DE3 platform, any hardware development kit is possible. Figure 5 displays the stacked DE3s and HDMI daughter cards which form a 3 x 3 Full HD HDMI frame split processor. This is suitable for TV Wall applications.

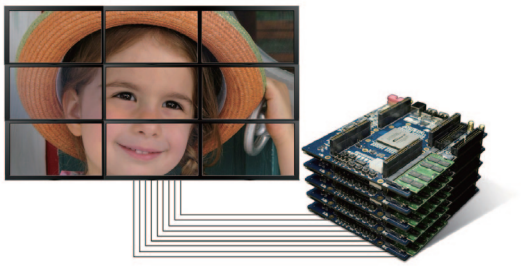

Figure 5. Stacked DE3s and HDMI daughter cards forms a 3 x 3 TV wall

REFERENCES

[1]. Recommendation ITU-R BT.709-5, International Telecommunication Union, Apr. 2002.

[2]. High-Definition Multimedia Interface Specification Version 1.0, HDMI Licensing, LLC, Dec. 2002.

[3]. High-Definition Multimedia Interface Specification Version 1.3, HDMI Licensing, LLC, Jun. 2006.

[4]. High-Definition Multimedia Interface Specification Version 1.4, HDMI Licensing, LLC, May 2009.

[5]. "DE3 User manual," Terasic Technologies, Hsinchu, Taiwan.

[6]. Nuno-Maganda, M.A. "Real-time FPGA-based architecture for bicubic interpolation," in Reconfigurable Computing and FPGAs, 2005, paper 10.1109, p. 8.