Holographic Display System Based on FPGA and DLP Technology

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Abstract — We describe a light field display able to present 3D graphics to multiple viewers around the display. The display consists of a high-speed DLP projector, a spinning mirror and FPGA circuitry to decode specially rendered HDMI video signals. The display uses a customized Nios II processor to rendering 1440 images per second 3D graphics, projecting onto spinning display with 3.75 degree separation up to 15 updates per second.

Keywords — Holographic Display, FPGA, DLP, NIos II, HDMI

I. INTRODUCTION

The rapidly emerging technology in recent years on multi-color, large-screen, high-definition projection system and other new technologies are being actively explored. A new projection manifestation method is being searched to address the needs of the various areas of the three-dimensional display. However, the existing commercial 3D TV still remains in the original binocular "pseudo-three-dimensional" technology. Long-time view can cause visual fatigue and even physical discomfort such as dizziness due to fixed perspective of traditional 3D TV view angle and fixed eye's focal point. Therefore, we are looking forward to a technological revolution to change the drawbacks of traditional 3D display technology so that images could be observed from any angle from the corresponding three-dimensional image.

For this purpose, we have designed and implemented a three-dimensional holographic imaging system. the system is a composition of a holographic image generator, DLP (Digital Light Processing) projector and a high-speed rotating screen. Holographic image generator is the signal source of a DLP projector, real-time and high speed three-dimensional holographic image is sent to the DLP projectors; Under the control of the holographic image generator, the micro mirror array (Digital Micromirror Device, DMD) of the DLP projector reflect light to the rotating display; Angular velocity of high-speed rotating screen is in accordance with the requirements of specific rendering algorithms, to ensure the correct projection frame is synchronized with the high-speed rotating screen. Thus, providing a new direction for three-dimensional, 360-degree, full range static and dynamic images projection technology. The subject being studied differs from traditional 3D TV that utilizing human eye binocular visual posed effect; observer can view the corresponding three-dimensional image from any angle. The designed is based on light reflection to implement a holographic three-dimensional effect, to give a real sense of three-dimensional.

From a market point of view, the design will enjoy a wide range of applications from consumer appliances, entertainment, to medical industrial design as well as scientific research and others. In the early stages of development, this can be applied to high-tech products advertisement. Imagine when Altera announce a now produce

at a conference hall, the light slowly goes out, the center of circular podium emerges a three-dimensional scene of a well fabricated 22nm FPGA, each angle demonstrate a different scenario, the chips then breaks up layer by layer, displaying its shocking internal structure. After the maturity of this technology, especially when the high-speed rotating screen is replaced by other light controlling device, will completely change how mankind access visual information and the traditional flat panel displays will be replaced.

Of course, a long way to go is ahead of us to really implement the technology. We hope that this topic can be used as a guide, diversify our thinking and to explore a more convenient and efficient three-dimensional displaying methods. We believe that the rapid development of integrated circuit and the use of low-power, high-performance optical path controlling technology in holographic display must become a hot area of future technological search and marketing.

In device selection, we choose Terasic DE3 platform equipped with the ALTERA Stratix III family EP3SL340H1152C2NFPGA FPGA chip. The chip contains up to 338,000 logic cells and high-speed external memory interface supporting DDR, DDR2, DDR3, and as much as 1104 user defined interface to meet the demand for high-speed, multi-IP library support in prototype development, suitable for high-speed and large-amount data processing requirements.

II. Functional Description

This system create a holographic image by splice 2D images, we need present a real object visually around all 360 degrees, so the system must process a lot of data in a very short time. The human eye to do a sampling system, based on previous studies, when the sampling frequency is 24 fps and above, we see better image continuity. If the Frame rate is higher the Visual effect is better. If around the 360 degrees output a image one by one degree, and fulfill the need of human eye (above 24 fps), so the system need output 8640 frames in a second (360 * 24 = 8640). It is difficult to complete for a normal projector, the DLP projector system also can't finish this task. Our DLP can only output maximum 4000 fps. So we calculate a balance frame rate number is 1440 fps. And in this fps, the Image quality and the system Performance can be balance. That need us sampled once every 3.75° in the horizontal sampling of the real object 360 degrees, that is, a circumference of 96 samples. Each angle giving the eye within second output 15 frames, the system effect is nice and it looks like a real object. Now more popular on the market of image transfer protocol VGA, DVI, HDMI, they support each pixel 16 \ 24 \ 32-bit color image transmission. Today, any video transmission interface can not be achieved within 1 second transmission of thousands of frame images, the frame rate of the video transmission interface protocol typically between 60 to 80 fps. However, if the use of Each pixel contains 24-bit chroma, sacrificing color, improve the speed, adding a different frame of information in each bit in the frame rate of 60 fps can be transmitted in seconds 60 * 24 = 1440 frame images, can greatly speed up the the ordinary transfer port transmission rate. The TI Lightcrafter development board has save a lot of work, especially at the decoder side, the on-board FPGA has complete the realization of image compression decoding, which been said before. we need to do is to transmit correct video stream via HDMI transmission protocol to the development board, so you can get on the DLP image decompression.

First need to sample imaging object, the object may be the reality of the object can also be rendered 3D computer model. Shooting around the object in the same horizontal plane, every 3.75 ° take a picture, so shooting finished after a week, you can get 96 images of 3D objects. Next binarize the color pictures taken. Compressed into 24 binarized images captured using the HDMI transfer protocol, in each pixel of the frame

constituted by the 24-bit. In order to enhance the clear view of the binarized image, we use the Dithering algorithm, the binarized image obtained by the MATLAB superimposed every 24 binarized images, composed of a new 24-bit color photographs. These original 96 frames become the 4 images by processing.

These images through a computer sequentially stored in the SD card, so that the CPU make these images are sequentially dump DDR2 memory to generate a video stream to take advantage of high-speed access speed of the DDR2 memory. Then the processed video stream input to the HDMI control module, a 608X684 resolution of the frequency of 60 Hz video stream is output to the projector. When the screen out of the projector and the rotational speed of the screen, can be matched. we will obtain a clear stereoscopic image.

III. Performance parameters

The system is a holographic image player, which consists of Image Pusher, High-speed Rotating Screen and DLP projector. The holographic image has a 360-degree viewing angle, so you can watch the 3D image at any direction in horizontal. The image of a resolution of 608*684 pushed by the Image Pusher to the DLP projector in the rate of 1440 fps. So image can update in every 3.75°, and made the frame rate to 15 fps in each angle.

Development platform is DE3, produced by Terasic Technologies, Inc. Because the system include a large number of computing and data transmission. The platform has an Altera Stratix III EP3SL340H1152C2N FPGA, a wealth of on-chip resources, and the speed class is C2, the performance can meet our design requirement.

IV. Design Structure

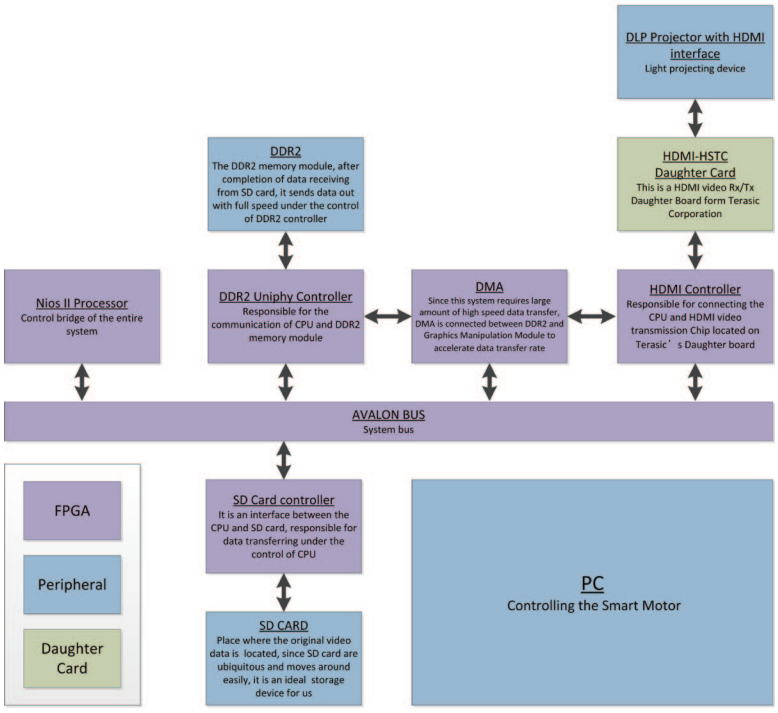

Figure 1. Block diagram

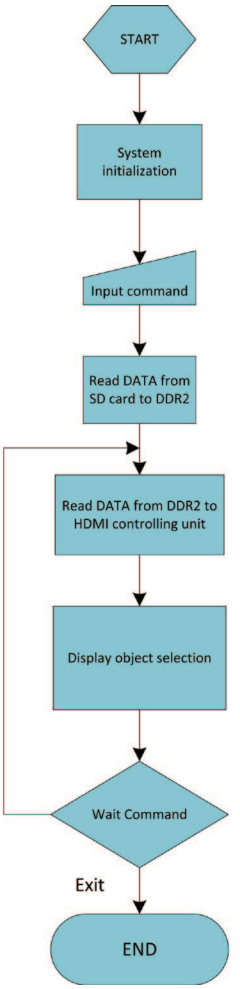

Figure 2. Flow chart

V. Design Method

This design is mainly constituted by Image Processor and Pusher, High-speed Rotating Screen and DLP projector. The FPGA achieve the part of Image Processor and Pusher.

The Image Processor and Pusher constituted by NIOS II processor, SD CARD, SG DMA, THDB-HDMI, DLP and the other hardware. The software includes BSP, driver and other algorithm code.

The process of the design is as follows:

[1]. System Requirements.

[2]. Module division.

[3]. Function implementation of each module, module testing and integrated IP core.

[4]. System testing, NIOSII software design.

[5]. System debugging and verification.

Here we will detail the design process of our system:

[1]. System Requirement Definition: We verified the system requirement through group discussion and meeting. Because 3D image system require large memory resources and high-speed processing to ensure real-time and synchronize, so the requirement is :

- Daughter board with HDMI interface, which used to translate the image date, processed by FPGA, to the DLP via HDMI cable.
- 1GB DDR2 memory, because a holographic image in the horizontal plane includes 96 pictures, this is a large amount of data.
- SD-card, which used to store the image to be displayed.
- DLP, the LIGHTCRAFT series DLP of TI Co. is so fast to meet our requirement of project in a speed of 1440 fps. There is also an Altera FPGA on it.

[2]. Module division: The whole system is divided into the SD CARD Data Storage module, the DDR2 Data Storage module, Image Data Processing module, SG DMA module and HDMI module. And defines the interfaces between the various modules. Decide to use a NIOSII processor to control the data flows. The details refer to our design configuration diagram.

[3]. Function implementation of each module, module testing and integrated IP core: We completed the module one by one. And test them individually. Finally to integrate the IP cores by the avalon bus in the QSYS tools.

[4]. System testing, NIOSII software design: First, use the QYS tool to connect the IP cores together by avalon bus. Second, built our software project and BSP in the NIOSII SBT for Eclipse. Third, add the driver of each module to the NIOSII project and programming. Finally, our system is built up. But you know, a new system is always having a lot of bugs. So we used about a month to debug. During this period, we used Modesim to simulating; used SignalTap tools to observe the waveform, and used TimeQuest Timing Analyzer tools to add timing constraints.

[5]. System debugging and verification: In this period, we have to test and adjust the performance of the entire system, such as adjust the resolution to achieve a better result.

VI. Design Features

Holographic projection is an emerging technology; a wide range of applications is not enough. Universal realization method is use computer to control multiple projectors to imaging in a reflection. Our method is the lowest cost and trying to design a custom dedicated chip to replace the computer.

EP3SL340H1152C2N chip is a high-end product of ALTERA Company. On-chip resources are very rich, and the speed grade is C2. This feature is appropriate to meet the requirement of high-speed data processing. What's more, DE3 platform has a DDR2 interface, which gives a rich memory space to the huge data. Last but not least, the Terasic HDMI-HSTC daughter board is so convenient that we can pusher the image to the DLP projector.

CONCLUSIONS

This contest has a deeply meaning for us, through the design and implementation of a customized system, we have mastered the full set of FPGA design methods, enforced information collection skills, team collaboration innovative thinking, and hard-working spirits.

First, in the system requirement analysis phase, due to the harsh demanding requirements of our system, we did a full survey of all types of ALTERA FPGA devices and Terasic development board and ultimately decided to use Terasic DE3 board with the equipment of STRATIX III family FPGA as our platform. In addition, the selection of the HDMI daughter board and DLP projector have cost a lot of time and effort, meanwhile we also gained a lot of experience in equipment selection resource utilizations.

Secondly, in the process of module design, we refer to the many altera provided IPs, many of the IP cores we need could be found at the official website of the Altera, through simple modifications can we quickly integrate into our system, which greatly reduced our efforts and time in code design. In system synthesis process, we used QSYS a tool, with it's easy to use graphical interface, with only mouse to drag can we to complete the connection between the various modules. Nios II SBT for eclipse tools also provides us with a friendly software development environment to facilitate software development.

Again, I deeply appreciate the longer perfect system must have a variety of bugs, but often the system of testing and bug fixes time is much longer than the development time. With SignalTap tools help, we observe a waveform diagram of the interface data observed every moment needed, and ultimately find the root of the problem. and TimeQuest Timing Analyzer tool allows our system to be able to meet our demanding timing requirements.

Finally, we do appreciate the terasic company's technical support; enthusiastic detailed answers to us when we met the HDMI daughter board cannot

support of our DLP 608 × 684 resolution issues. Though Entire project, the tacit understanding between the members of our team has improved, and also develops our common division of the ability to discuss and resolve the problem. In the commissioning phase of the project, we encountered a lot of problems, thanks to the guidance of our instructor Cao Jian, help us solve many problems. Thank all who concern and support of our project, without your help our project would not be so smooth completed.

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