Development of EEG-based Intelligent Wheelchair Based on FPGA

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Abstract - In this paper, an intelligent wheelchair control system which can provide auxiliary help for disabled patients based on BCI is proposed. This system is based on 90% of normal brain function people whose Dwave amplitude of EEG can be significantly enhanced in the short eyes closed. We place two detection electrodes on the occipital and forehead of the brain, pre-amplify the detected signal, and then after a series of signal processing, we can simply and easy control the movement of the electric wheelchair and do not need training or only a small amount of training. Through the TI's ADS1198 analogy front-end circuit, we realize EEG acquisition, amplification, isolation and data pre-processing. Data is processed in the Nios II environments. Finally, the system controls the YIFUCON's wheelchair KB5618 in accordance with the appropriate action.

Keywords — EEG, Nios II, KB5618, ADS1198, wheelchair

I. SYSTEM DESIGN

The United Nations issued that the world aging population is accelerating. The next 50 years, the proportion of the population over the age of 60 is expected to double. Moreover, people with disabilities caused by a variety of disasters and disease have increased year by year. They suffered from different degree of disability, such as walking, vision, hands, and language. At this situation, in order to improve the life quality of the elderly and the disabled people and help them back into social activities, a motion assistance system is needed. Presently, some countries like the United States, Germany, Japan, France, Canada, Spain and China have began to study the intelligent wheelchair which could have a memory map, obstacle avoiding function and walking automatically via user commands.

The smart wheelchair also known as the intelligent wheelchair mobile robot is the electric wheelchair that applies the intelligent robot technology, which integrates a variety of fields including robot navigation and positioning, pattern recognition, multi-sensor fusion and human-machine interface (HCI) involving mechanical, control, sensors, artificial intelligence, communications technology, Its motion achieves in a almost no radius of gyration of the real meaning of the omni-directional motion. Especially, it can adjust position while keeping the body posture unchanged. It is a great step forward for people with weak walking ability, because it makes it posible for the disable people to access to the place they want without others' care. At the same time, If we design out more function (for example, the humanity of the HCI, navigation and obstacle avoidance function) in a wheelchair, this kind of wheelchair will be more promising. The developed

intelligent wheelchair can not simply copy the traditional design methods and theories of the robot. And it must truly set the "people" as the center, focusing on the issue of intelligent humancomputer interaction. Unlike industrial robots and electric machines to achieve a specific production tasks, the intelligent wheelchair, all of its service behavior must interact with human to achieve the "man-machine-aware interface", so that a wheelchair can 'see', 'hear' and able to integrate a variety of channels of information to perceive the external environment. Human can interact with intelligent wheelchair in a more convenient and natural way such as facial gestures, expressions, gestures and voice and etc. Besides, they can transmit their own knowledge and experience to the wheelchair. It is worth noting that if humancomputer interaction issues are not properly resolved, it will become a bottleneck restricting to the development of intelligent wheelchair.

Since Britain started to develop an intelligent wheelchair in 1986, many countries began to allocate more funds to study the intelligent wheelchair, such as US MIT WHEELESLEY project, the project of the University of Ulm in Germany MAID, the European Union TIDE project. Intelligent wheelchair research started late in China, and the complexity and flexibility of the structure have a certain gap when compared with abroad, but there also exist some smart wheelchair close to the international advanced level of technical qualification according to its own characteristics. The domestic research units mainly are the Chinese Academy of Sciences Institute of Automation, National Chung Cheng University, Taiwan Department of Electrical Engineering, Shanghai Jiaotong University. The third Military Medical University. Their researches have made some achievements. However, there are still some problems. It is suggested that the trends of intelligent wheelchair research in the future concentrates on user-friendly, modularity.

In our study, the Nios II embedded processor was used. Compared with other processors like MCU, DSP, ARM, Nios II soft-core processor has the following characteristics. Firstly, SOPC proposed by Altera is a flexible, efficient SOC solution. It integrates Nios II processor, memory, the I/O port and other functional modules into an FPGA which is a programmable on-chip system. It has a flexible design approach and provides a number of available IP cores that can be cut, expanded, upgraded. Secondly, Nios II is a kind of soft-core embedded developments. It is flexible, high-performance, low-cost, long life cycle and provides a lot of technical documents and examples of development. If you are expert, you can design anything you can imagine with FPGA. This is the greatest significance of the Nios II. Nios II supports MicroC / OS-II, uClinux and other real-time operating systems, and also supports lightweight TCP / IP protocol stack, as well as ".Zip' files system. Nios II allows users to add custom instructions and hardware acceleration unit, and transplant custom peripherals and interface logic seamlessly. It improves the performance as well as facilitates the design for user. Finally, the development of embedded systems on FPGA in Altera is in forefront of the world all the way.

In summary, our design is user-oriented terminal design and provides the aging population, the young people and children (such as accidents, disability, congenital diseases) who rely on technology to sustain life, the advanced cancer or AIDS patients and special healthy crowd (new baby, pregnant women) a convenient and suitable operation family-intelligent wheelchair controlled by EEG.

II. FUNCTION DESCRIPTION

In this paper, an Intelligent wheelchair control system which can provide auxiliary help for

disabled patients based on BCI is proposed. This system is based on 90% of normal brain function people whose α wave amplitude of EEG can be significantly enhanced in the the short eyes closed. We place two detection electrodes on the occipital and forehead of the brain, pre-amplify the detected signal, and then after a series of signal processing, we can simply and easy control the movement of the electric wheelchair however do not need training or only a small amount of training. The system can be extended to more complex multioption of real-time control system. Through the corresponding experiment, we can prove this based on α brain - machine interface system can be realized, and the system has the potential application value. Through further integration and portability, and the configuration of an appropriate information feedback LCD, we can develope out a specifical new assistive products for those with systemic severe paralyzed but mind functioning is regular.

The system hardware consists of the DE2 development platform, TRDB-the LTM LCD screen, EEG amplifier, wheelchair model. The system can be divided into three functional modules: EEG acquisition, amplification and preprocessing module; EEG signal processing and control module; LCD display, and humancomputer interaction and wheelchair control module.

1) **EEG acquisition, amplification and preprocessing module:** We use Texas Instruments (TI) company's fully integrated analog front end (AFE) chip ADS1198 as the core analog front-end circuit for EEG acquisition, amplification, isolation and other pretreatment operations.

2) **EEG signal processing and control module:** This is the part of the algorithm of the system, also the core functionality of the system. We take advantage of the Nios II processor and powerful computing power of a PC, and the most of the algorithm is C code. 3) LCD display and human-computer interaction module: We use a digital touch panel LCD TRDB-LTM provided by Altera Corporation and some buttons as display and human-computer interaction respectivly. We use the IP core to add to Avalon to driver the LCD. Button, we choice interrupt mode to trigger reset, start, and closing functions of the control system.

4) Wheelchair control module: We use Yifucon KB5618 wheelchair, and then give the control signal to the wheelchair control system we can control wheelchair go straight, turn left, turn right.

III. PERFORMANCE PARAMETERS

This system utilizes the trait of amplitude value of α wave on the cerebral cortex will increase when eyes close. We provide a simple and reliable electronic device switch control method, and we have done some exploratory expansion. We use the assessment principles in its design of the user interface: Effective Human-Computer Interaction Principles by Ben Shneiderman, founder of the Human-Computer Interaction Laboratory of the University of Maryland to measure the BCI system performance assessment:

A. The time of learning to use the system

This system explores and uses the trait of amplitude value of α wave on the cerebral cortex will increase when eyes close, and then finish the control system.And more than 90% of the population has this trait, so almost no learning or only a very short time of learning for us to use this system.

B. The execution speed of the system

It's real-time online operation, relatively fast. Despite the individual differences, the time required to trigger switch is still relatively short, execution speed is faster.

C. The errors will occur, and the kind of error

This system depend on the data collected from brain electric signal to decide the direcrion for the wheelchair to turn such as left, right and go straight ahead. Due to the complex brain electrical signals and the different levels of testers' training, turn left will be sentenced to turn right and on the contrary, turn right or go straight also mistaken for the other two actions. Accordingly, there are six types of error, the average error rate of approximately 20%, with a further improvement of the design and the increase of the frequency and duration of trainer's training, receiver error rate will be greatly reduced.

D. How long can users keep this knowledge

A long time, because almost do not need training and repeatability is very strong.

E. The user's comfort and satisfaction

Electrode small, easy to install, and in places outside the line of sight, and from the appearance it's equivalent to wear an ordinary hat,. It can reduce the visual signals of the disabled, so it can avoid patients' self-confidence and self-esteem to be hurt.

IV. DESIGN STRUCTURE

A. Hardware system design diagram

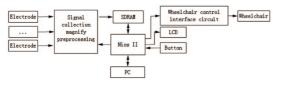


Figure 1. Hardware system design diagram

B. Software system flow chart

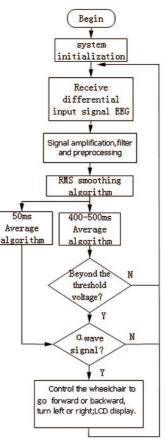


Figure 2.Software system flow chart

V. DESIGN METHOD

A. The design of the hardware platform

1) EEG signal acquisition, amplification and preprocessing module

The system uses the core of TI's ADS1198 as analog front-end circuit. ADS1198 has the following main features :

 8-channel 16-bit ADC converter chip, the sampling frequency is 125sps ~ 8ksps.

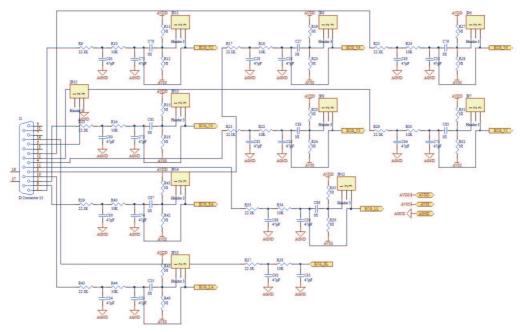


Figure 3.ADS1198 analog front-end input circuitry

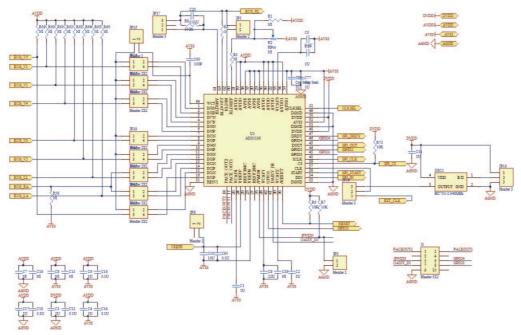


Figure 4.The core of the ADS1198 analog front-end circuit

- Each channel has programmable amplifier, whose magnification is adjustable from 1 to 12 times; when CMRR>100dB, input impedance is approximately 10 M Ω .
- It contains the right leg driver amplifier and Wilson central terminal.

According to ECG or EEG patterns of specific applications, the MCU makes configuration

multiplexer (MUX) the internal input end (INPUTS, RLD) on or off, so that programmable amplifier (A1-A8) magnification and AD converter(ADC1-ADC8) sampling frequency. When the chip completes a conversion, Data Ready pin goes low to notice MCU through the SPI bus to read data.

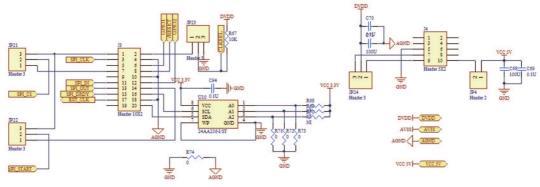


Figure 5.The interface of ADS1198 analog front end and DE2 circuit

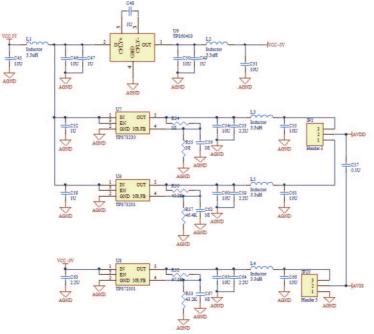


Figure 6.ADS1198 analog front-end power supply circuit

- [1]. ADS1198 analog front-end input circuitry It contains the second-order passive low-pass filter and limiter circuit and play a role in the elimination of high-frequency interference and overvoltage protection. The low pass cutoff frequency is 30 kHz and the amplitude of the voltage range is \pm 700 mV.
- [2]. The core of the ADS1198 analog front-end circuit
 It makes configuration of the ADS1198 peripheral pin, and leads to the control port and SPI command input and data output port.
- [3]. The interface of ADS1198 analog front end and DE2 circuit This completes cohesion analog front-end circuit and DE2 board, so that the brain electrical signals transmit through the circuit to the DE2 board for data processing.
- [4]. ADS1198 analog front-end power supply circuit This contains the TI's TPS60403DBVR, TPS73230DBVR, TPS72301DBVT and TPS73201DBV. These polarity converter and voltage regulator chips converter +5V (DE2 panel) to -5V, +3.0 V,-2.5V and +2.5 V to meet the ADS1198 power supply requirements.

2) The wheelchair and its control module

We choose the YIFUCON's wheelchair KB5618. The wheelchair has two driving wheels (right and left) before passive wheel plus. The rotation of the rear wheel is controlled by two DC motors. The motor controller uses the PG controller. Through communication with PG controller we can control the speed and direction of the wheelchair.

Control system: The British PG controller accelerates smoothly, jitter-free, downhill automatic transmission, energy saving. Through communication with PG controller we can control the speed and direction of the wheelchair.

PG controller: The start of the controller is a high level of 5ms. Both the opcode and data bit is 8bit binary.

Opcode and the format of the data bits: 1 start bit, 8 data bits,1 parity bit and two stop bits. The start bit is low electrical level enabled.The stop bit is two high electrical levels enabled.

Control signal packet format: 5ms HIGH + stall control data +8 bit receiver when the data (transmission 0) + the data about going forward or backward +the data about turning right or left+ checksum data;

The front and rear, and left and right in controller constitute a Cartesian coordinate system. Through the different x and y values, we can achieve any angle of rotation, and we can adapt to different terrain and population adjustment stalls. The wheelchair has a good brake system. The brake signal is generated by the controller to control the motor brake.

We use the FPGA to complete the package of data interface, so that the follow-up call is very convenient. In order to obtain the speed and direction information, we will analyze the EEG data obtained after processing in the FPGA, a certain format of a packet transmitted to the PG controller, completed by the PG controller for the motor control. Taking into account the human EEG sampling time differences, in order to prevent continuously appearing multiple times in one direction deflection, we set brake motors to stop wheelchair walking. So we can guarantee security.

Through the communication with the PG controller, we can easily read the battery information. And we can also read the failure information, including motor failure, brake failure. So we can facilitate the overhaul of our wheelchair easily.



Figure 7.YIFUCON's wheelchair KB5618

3) LCD image display and interactive modules

Most BCI systems need feedback. The most common form of feedback is cursor control. subjects move the cursor to the specified target location, only use the up / down or left / right two sets of commands. Cursor is in the middle of the screen at first, and then each section of the cursor meets the target location or the opposite position. When it comes to the target location, the cursor will blink, indicating success. This feedback can enhance the confidence of the subjects with the idea of operating the cursor. Cursor control provides persistent feedback, so the subjects are able to see their own ideas driving the cursor on the mobile, such as the wrong direction can promptly adjust. For BCI systems, particularly those based on the operating conditions BCI systems, feedback is necessary, subjects need to know which ideas can move the cursor which direction movement.

The LCD image display is actually a feedback platform. The image displayed on the " $\uparrow \downarrow \leftarrow \rightarrow$ ", respectively correspond the subjects' controling the wheelchair front, rear, left, and right directions. Combining with the feedback of the success "Success!" we can remind the operator to successfully carry out the operation. The purpose of doing so is to enhance the stability and accuracy of the system in order to focus the attention of the subject and excite continuing experiments power.

The system's LCD display module is TRDB_ LTM, which is provided by Altera Corporation.

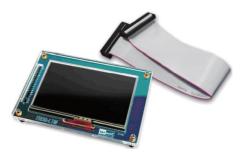


Figure 8.TRDB_LTM uniform look

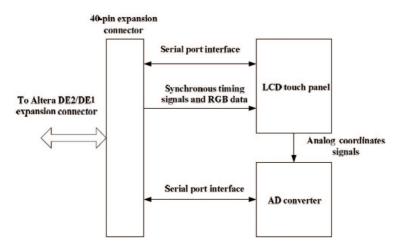


Figure 9.TRDB_LTM overall diagram

TRDB_LTM mainly includes LCD touch panel module AD converter and a 40-pin expansion signal interface module. 40-pin expansion signal interface is used to connect DE2/DE2_70/ DE1 development platform reserved for 40-pin expansion port; LCD touch panel module from the FPGA AD converter input control signal and image is displayed on the LCD panel; the coordinates of the touch point value is exported reserved interface of the FPGA to achieve the effect of touch control.

In addition, the system uses the keys on the DE2 to select interrupt mode, trigger control system reset, start up, and shut up and so on.

4) SOPC Builder Construction and QuartusII Hardware Structures

This is SOPC structure of our system.The system clock uses 100M, which is produced by external clock (50M) PLL multiplier. Add cpu, tri_ state_bridge, cfi_flash, sdram, epcs_controller, jtag_uart, uart, timer, lcd_16207, led, button_pio, DM9000A, VGA, ISP1362, ADS1198_DRDY, ADS1198_SPI, ADS1198_RESET, ADS1198_ START, ADS1198_DATA module components, etc.

Target		Clock Settings						
Device I	Family: Cyclone I	Name		MI				
		clic			External		100	
		c8k_50			External		58.0	
Joe .	Module Name	Description	Clock	Dase	End	RO		
V	🖽 cpu_0	Nos I Processor	cik	# 8x8150100	0 0401501766			
	E tri_state_bridge_0	Avalon-MM Tristate Bridge	cik					
	E cfi_flash_0	Flash Memory (CFI)	cik	· 0x0140000	0 Oz017ffffff			
	E sdram_0	SDRAM Controller	c8c_58	# 8x808000	11111100g0 0			
	E epcs_controller	BPCS Serial Flash Controller	elk	# 0x01b0100	0 Oz01b01fff			
	E jtag_uart_0	JTAG UART	elk	# 0x01b0215	0 0m01b02157	→ ••		
	E uart_0	LIART (RS-232 Serial Port)	clk	# #x#1100200	0 0x01b0201f			
	E timer_0	Interval Timer	clk	· 0x0110202	0 0x01b0203f	⊢ 6		
	E timer_1	Interval Timer	cik		0 0x0150285f	→ •		
	E lcd_16207_0	Character LCD	cik		0x0150288f	T		
	E led_red	PIO (Parallel I/O)	cik	· 0x0110201	0x0150209f			
	E led_green	PIO (Parallel I/O)	elk	· 0x011020s	0x01b020af			
	E button_pio	PIO (Parallel I/O)	elk		0 0x0150205f			
	E switch_pio	PIO (Parallel I/O)	clk		0 0x01b020cf	T		
	E SEG7_Display	SEC7_LUT_8	clk		0 0x01502163			
	E sram_0	SRAM_1688_512K	clk		11111AIGu0 0	1		
	E DM9000A	DM9000A	cik		8 0x01b0215f			
	E 15P1362	KSP1362	cik		0x0150204f	H		
	E VGA 0	Binary_VGA_Controller	cik	· 0x0180000	a Oz019ffffff			
	E Audio_8	AUDIO_DAC_FIFO	elk		4 0x01502167			
STATES STATES STATES STATES STATES	E SD_DAT	PIO (Parallel I/O)	elk		0 0x015020af			
	E SD_CMD	PIO (Parallel I/O)	clk		0x01b020ff			
	B SD_CLK	PIO (Parallel I/O)	cik		0 0x01b0210f	1		
	ADS1198_DRDY	PIO (Parallel UO)	clk		0 0x01b0211f			
	E ADS1198_SPI	SPI (3 Wire Serial)	cik		a 0x0150207f			
	E ADS1190_RESET	PIO (Parallel UO)	cik		13150410#0	_		
	E ADS1198_START	PIO (Parallel IIO)	cik		0x0150213f			
	E ADS1198_BATA	PIO (Parallel I/O)	elk	· 0x0150214	a 0x0150214f			

Figure 10.SOPC Builder interface

Then, assign pin and compile in the Quartus II to generate hardware .SOF file.So the hardware platform portion of the works will be designed.

clk	
reset_n	
	out_port_from_the_ADS1198_DATA[150
in_port_to_the_ADS1198_DRDY	
	out_port_from_the_ADS1198_RESET
MISO_to_the_ADS1198_SPI	MOSI_from_the_ADS1198_SPI SCLK_from_the_ADS1198_SPI
	SS_n_from_the_ADS1196_SPI
	out_port_from_the_ADS1198_START
iCLK_18_4_to_the_Audio_0	oAUD_BCK_from_the_Audio_0
CCK_10_4_t0_ble_Abblo_0	oAUD DATA from the Audio 0
	oAUD_LRCK_from_the_Audio_0 oAUD_XCK_from_the_Audio_0
ENET_INT_to_the_DM9000A iOSC_50_to_the_DM9000A	ENET_CLK_from_the_DM9000A ENET_CMD_from_the_DM9000A
	ENET_CS_N_from_the_DM9000A
	ENET_DATA_to_and_from_the_DM9000A[150] ENET_RD_N_from_the_DM9000A
	ENET_RST_N_from_the_DM9000A ENET_WR_N_from_the_DM9000A
OTG_INT0_to_the_ISP1362 OTG_INT1_to_the_ISP1362	OTG_ADDR_from_the_ISP1362[10] OTG_CS_N_from_the_ISP1362
0.0_m11_t0_m6_t0P1302	OTG_DATA_to_and_from_the_ISP1362[150]
	OTG_RD_N_from_the_ISP1362 OTG_RST_N_from_the_ISP1362
	OTG_WR_N_from_the_ISP1362
	out_port_from_the_SD_CLK
	bidir_port_to_and_from_the_SD_CMD
	bidir_port_to_and_from_the_SD_DAT
	oSEG0_from_the_SEG7_Display[60]
	oSEG1_from_the_SEG7_Display[60]
	oSEG2_from_the_SEG7_Display[60] oSEG3_from_the_SEG7_Display[60]
	oSEG4_from_the_SEG7_Display[60]
	oSEG5_from_the_SEG7_Display[60]
	oSEG6_from_the_SEG7_Display[60] oSEG7_from_the_SEG7_Display[60]
iCLK_25_to_the_VGA_0	VGA_BLANK_from_the_VGA_I
	VGA_B_from_the_VGA_0[90
	VGA_CLK_from_the_VGA_ VGA_G_from_the_VGA_0[9.1
	VGA_HS_from_the_VGA_U
	VGA_R_from_the_VGA_0[90 VGA_SYNC_from_the_VGA_1
	VGA_VS_from_the_VGA_
in_port_to_the_button_pio[30]	
	LCD_E_from_the_lcd_16207_0
	LCD_RS_from_the_lcd_16207_0 LCD_RW_from_the_lcd_16207_0
	LCD_data_to_and_from_the_lcd_16207_0[70]
	out_port_from_the_led_green[8
	out_port_from_the_led_red[17
	zs_addr_from_the_sdram_0[11
	zs_ba_from_the_sdram_0[1t zs_cas_n_from_the_sdram_
	zs_cke_from_the_sdram_
	zs_cs_n_from_the_sdram_ zs_dq_to_and_from_the_sdram_0[15!
	zs_dqm_from_the_sdram_0[10
	zs_ras_n_from_the_sdram_ zs_we_n_from_the_sdram
	SRAM_ADDR_from_the_sram_0[170]
	SRAM_CE_N_from_the_sram_0 SRAM_DQ_to_and_from_the_sram_0[150]
	SRAM_LB_N_from_the_sram_0
	SRAM_OE_N_from_the_sram_0 SRAM_UB_N_from_the_sram_0
	SRAM_UB_N_trom_the_sram_0 SRAM_WE_N_from_the_sram_0
in_port_to_the_switch_pio[170]	
	select_n_to_the_cfi_flash_
	tri_state_bridge_0_address[210 tri_state_bridge_0_data[70
	tri_state_bridge_0_read
	write_n_to_the_cfi_flash_

Figure 11.In SOPC Quartus II generated module

B. The design of the software platform

The collected EEG went through a preamplifier, 50Hz notch, 30Hz range signal preprocessing, and the subsequent processing is done in software Nios II platform. The entire software design process: receive differential input signal after pretreatment, and then reserve α wave through the main frequency band of the bandpass filter of 8 \sim 13Hz. After 10ms of the RMS smoothing algorithm,the signal is divided into two:one goes through 400

 \sim 500ms (varies) average algorithm, which is the main control path; another goes through a 50ms average algorithm, which is the auxiliary control pathway used to determine alpha wave control signal on the main path is α wave or a noise signal. The signal went through the first path and compared with the threshold voltage, If the signal is beyond the threshold voltage, compare with the signal which went through the second signal path to determine if it is α -wave control signal. If the signal is α -wave, control the wheelchair to go forward or backward, and turn left or right, and control the LCD to display feedback imformation. If the signal is not α -wave, re-read the differential input signal.

C. The determination of the system parameters

Experimental verification should be taken in the entire system: which mainly includes the collecting cap electrode position experiment, setting subjects ssthresh voltage trigger time experiment.The collecting electrode position experiment provides a basis for design of the electrode cap: values and illustrate voltage.The trigger time experiment is to determine the system parameters.

1) **Collecting electrode:** The α wave correspond with idle rhythm of the Visual area. Its frequency is 8 ~ 13Hz and the amplitude is approximately 20 ~ 100uV. It is most obvious wave of rhythmic brain waves.The d wave blocking phenomenon is the theoretical basis of the design. α wave is seen in all Scalp lead, especially the pillow District. Generally, for unipolar lead, showing the highest volatility is the pillow, followed by are the top and prefrontal. The early design select two traditional AgCl electrode to place in the occipital 01, T5 location. The collected EEG and earlobe reference electrode import preamplifier in differential mode. However, the electrode and the hair being in direct contact may cause the electrode junction skin impedance mismatch.What's more, the electrode is placed directly on the hair.For each acquisition, in order to improve the SNR of the signal, the electrode often soaks in physiological saline or contact area coats with a conductive paste, which is very inconvenient. So we designed a EEG acquisition cap.On the condition collected alpha wave has little effect on the system control, explore acquisition proud of some of the flexibility of changing the position of the electrode, making the signal acquisition easier, experimental easier cleaning. The specific approach is: earlobe reference electrode is constant, the collection the electrode by the Ol position of the occipital is moved to no hair forehead FPl, and the electrode positions are fixed in their hats, which simplifies the experimental procedure.Subjects' α volatility value in the 01 position compared to their α volatility value in the FPL position.Use EEGCollection software to collect and measure the α wave data in the steady state of the two positions, and then process it in MATLAB.

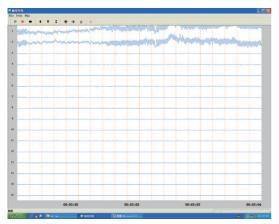


Figure 12. EEGCollection software collects EEG signals

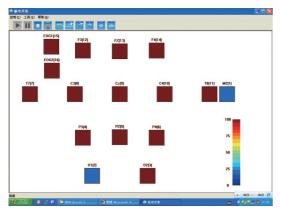


Figure 13. EEGCollection software detects electrode impedance

2) Threshold voltage: Each human subject distinguish from each other. The average of the RMS-DC averager voltage Vi imports one of the input terminal of a comparator, while the other input terminal is a predetermined DC threshold value of the threshold voltage Vth, which is manmade based on different subjects' EEG average Vqeo voltage value when they are calm and their eyes are open. Its value set relates to the stability of the system. If it was set too low, there will be a pseudo-positive potential—subjects are not quiet or close their eyes to generate a control signal, so that the input exceeded the threshold potential due to other interference and caused positive voltage, and the whole system is triggered. If it was set too high, it will cause the pseudo negative potential—subjects with eyes closed generate a control signal lower than Vth input potential, in other words, subjects has generated a control signal but has not triggered the normal system. By contrast, the harm of the pseudo negative potential is much smaller than the harm of the pseudopositive potential, so the threshold is set to avoid the emergence of the pseudo-positive potential. Vth is set as low as possible in the case of the least pseudo positively charged digit.

3) **Cycle time:** subjects operate instructions from the cycle lights on the control panel.The cycle time of looping the lights must match with the time subjects control signal generate, that is, when the light is on, subjects should close their eyes so that the generated control signal time coincides with the lights.While subjects opening eyes to control, cycle lights go out and subjects carry forward to the next control. Adjustable cycle lights cycle regulation is based on the the trigger time that experimenters control the signal.

VI. DESIGN CHARACTERISTICS

The design has the following features:

1) **Design concept:** This product used to help physical disability or aging can't walk crowd, as well as severe paralysis and even brain thinking population, bring these people the convenience of the action. Wearing the electrode cap, users just like put on an ordinary hat and do not have to worry about being ridiculed. Users do not need training or only a small amount of training and can control the movement of the electric wheelchair simply and easy, and the system can be extended to a more complex multi-option of real-time control system.

2) Product function: Through the experiment, we can conclude that this based on α brain machine interface system can be realized, and the system has the potential application value. Humancomputer interaction techniques for special groups or special purpose of development in intelligent wheelchair are different from general manual operation of the artificial intelligence technology. It became one of the key technologies (obstacle avoidance, self-positioning, human -computer interaction) of smart wheelchair, and also in a pivotal position in the development of intelligent wheelchair. Through further integration and portability, and the configuration of a appropriate information feedback LCD, we can develope out a specifical new assistive products for those with systemic severe paralyzed but mind functioning is regular.

3) Hardware design: SOPC make our design more simple and straightforward, each module can be done individually, but can easily integrate to form a system. we can embed in a system of multiple master devices (including AD, LCD) to achieve data transmission, greatly reducing the burden on the CPU; At the same time we can quickly upgrade hardware module, and an IP can be hooked up to the bus, this can't imagine when in chip-level structures of the SOC system in the past. All IP use Avalon bus architecture and adopt a unified synchronous clock.

4) **Software algorithms:** Our design is relatively complex, not only the design of the module, but also some complex algorithms embedded and the design difficulty is also the characteristics we must explain.

5) Extremely flexible Nios II processor-based EEG control intelligent wheelchair: we can configure and upgrade system quickly without having to replace the entire system platform according to the needs of different hospitals, community and family.

CONCLUSIONS

1) Through the study, we have deepened our understanding of SOPC, and acquireed a certain amount of experience in using Nios II CPU for embedded system development. The Altera SOPC gave us the strong design platform, so we can involve in hardware development, drive development and the application procedure development, and make system-level development faster and easier.

2) The project, we get start several months ago, gain is not only the final works, the more important is the experience. From the IP core design, the former after simulation, to optimize the application, we truly appreciate the design ideas, can be said we find the "feel" of the design. The development of embedded system tests our patience sincerely, and debug program is to spend most of the time, but it can benefit a lot.

3) Use embedded logic analyzer, SOPC Builder, nios ii IDE and DSP Builder to design product that can really speed up the development speed. Although individual division of labor is different, but we can learn all knowledge, we really appreciate the strength of the team.

4) Feel the deepest is NIOS and other embedded system difference in its flexibility. In the design process, we can see how a system formed from the lowest level of the realization of the design to the application layer transparently, and can strengthen our system consciousness deeply. This can not be compared to other embedded systems.

5) So far, our work still has a large space for development. For examples how to speed up the interface switching speed, how to enhance the performance of the DSP in the system, and to achieve a more accurate the biomedical signal waveform detection algorithm, we need to continue to work hard. 6) Finally, let us take this opportunity to thanks our teachers and friends for their help, thanks the competition organizers and judges for their hard work.Our lab will march on till victory is won.

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