# Autostereoscopy Image Display System

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*Abstract — The proposed work presents a naked eye 3D display technology programs, including the holographic video acquisition subsystem and 3D rectangular pyramid holographic imaging subsystem. The holographic imaging acquisition subsystem consists of two DE2-70 multimedia development boards which implement real-time multi-angle acquisition of data video and the compositing and output of holographic video; the 3D pyramid holographic imaging subsystem uses the see-though material as the display media. The output holographic video of HVAS is projected onto the respective sides of the quadrangular and then floated image with a 360° viewing range in the quadrangular pyramidal internal. Hence, this display program perfectly matches with the real environment and creates living and stunning visual effects.*

*Keywords — 3D Pyramid hologram, DE2-70, VIDEO PROCESS, NTSC, MULTI-PORT-SDRAM*

## I. INTRODUCTION

### A. Design Purposes

Human demand is the original motivation for the development of science and technology. In the field of display, 3D technology can truly reproduce the original appearance of world, giving us the immersive visual feast. The strong curiosity of human to restore the real world and the innovative spirit has been accelerating the development of 3D display technology. The current mainstream 3D display technology includes grating 3D display, integrated imaging 3D display, holographic 3D display and so on. The present work gives a naked eye 3D display technology programs, including the holographic video acquisition subsystem and 3D pyramid holographic imaging subsystem. The holographic imaging acquisition subsystem consists of two DE2-70 multimedia development boards which implement real-time multi-angle acquisition of data video and the compositing and output of holographic video; the 3D rectangular pyramid holographic imaging subsystem uses the see-though material as the display media. The output holographic video of HVAS is projected onto the respective sides of the quadrangular and then floated image with a 360° viewing range in the quadrangular pyramidal internal. So it matches the real environment perfectly and creates vivid, stunning visual effects.

### B. Application Scope

As a new display medium, the proposed work has a competitive cost and stunning visual effect. So it can be widely used in the information display occasions in business, teaching, medical, communications, industrial and agricultural production, such as, luxury, relics and art works displayed,3D film production, mold making and digital city map.

### C. Reasons for Using Altera Components

As we all know, there is a lot of rich multimedia, image processing hardware, software resources, teaching materials and a variety of illustrative

example on DE2-70 multimedia development platform. We thought it would be the ideal solution for handling multimedia applications. In addtion, in a very short time can we achieve our vision and complete the work.

Moreover, SOPC structure is quite flexible and can be customized on demand from the user peripherals of Avalon switch. We can adjust our own system requirements, such as multi-CPU, customized instruction set and hardware accelerators, in order to meet the designed performance requirements for both current and future.

## II. FUNCTIONAL DESCRIPTION

As shown for the high-level illustration of our hardware design and organizationin Figure1, the main function of the proposed work includes the browsing and acquisition for static holographic images, the synthesis and playing for the real-time holographic images.

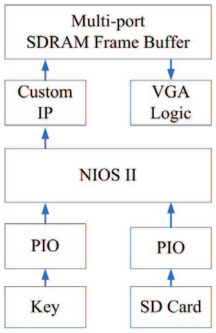


*Figure 1. Function block diagram of the static holographic image browsing*

With PIO core, we simulate how SPI communication reads the 3D pictures stored in the SD card. User-defined IP core sends the image data to multi-port SDRAM Frame Buffer, and then VGA control logic is responsible for reading and displaying data from the SDRAM Frame Buffer. KEY browses the next picture by PIO interrupt.

A function block diagram for acquisition, synthesis and playing real-time holographic image is shown in Figure2 as follows.

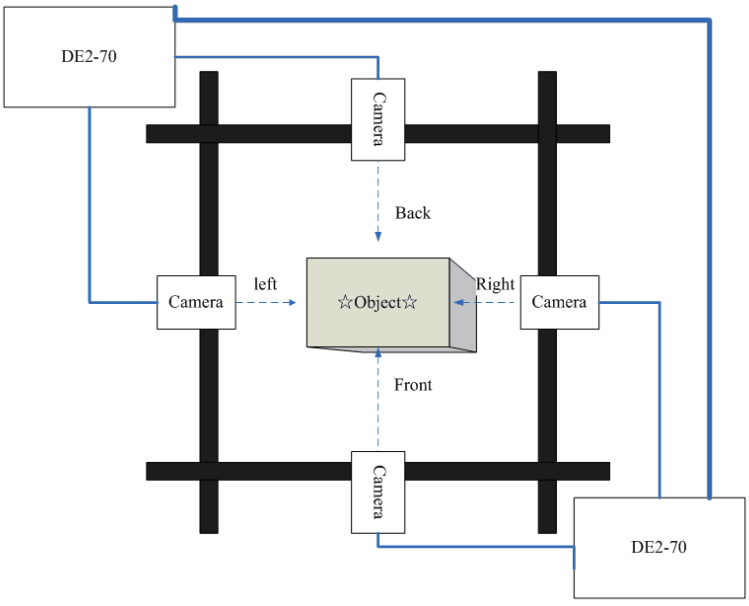


*Figure 2. Function block diagram of acquisition, synthesis and play real-time holographic image*

The two pieces of DE2-70 multimedia development boards work together, acquiring real-time four-channel camera data from all around, synthetizing 3D video source synchronously, and writing to multi-ported SDRAM Frame Buffer. The VGA control logic is responsible for reading data from the SDRAM Frame Buffer and then displaying them. While, KEY controls the display mode.

## III. PERFORMANCE PARAMETERS

### A. Image Parameters

- Input original image formats: NTSC system
- Output image formats: 30-bit RGB format
- Input image resolution: 640 × 480 pixels
- Image Color: 30-bit color
- Aspect Ratio: 4:3

### B. SD Card Parameters

- SD card capacity: 2GB
- SD card file system: FAT16 file system
- SD card read speed: 165.9KBps

### C. Auxiliary Resources

- SD card: 2GB Sandisk SD card
- Projection equipment
- Camera: Four 540 lines NTSC Television System
- Stent and background
- The rectangular pyramid holographic projection film

## IV. DESIGN ARCHITECTURE & DESCRIPTION

The principle of the proposed work includes the following two parts:

### A. Pyramid Holographic Film Frame

The 3D pyramid holography is shown in Figure 3.Each side of the pyramid is made of half inverse semi-permeable materials in the form of isosceles triangle and shows a 45 degree angle with the bottom surface. Hence each side functions to map the four different screen of 3D video source, respectively.

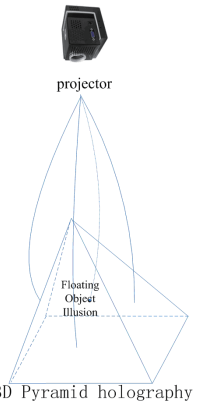


*Figure 3. The 3D rectangular pyramid holography*

### B. 3D Video Source

The production of 3D video source is one of the key of the whole system. By hardware and software means, 3D picture is broken down into four different side of the screen, proceed the frame synchronization synthesis, and then output the video. Four screens in a cruciform arrangement as shown in Figure 4 can realize the synchronous display for four sides of the 3D model screen.

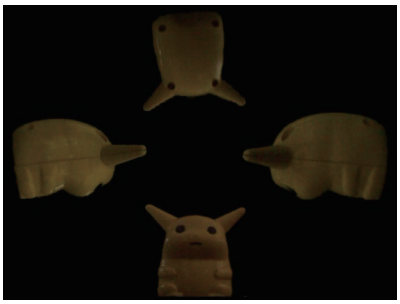

*Figure 4. 3D model screen is broken down into four different sides of the screen broken down in a cruciform arrangement*

1) Analyze DE2_70_TV module and grasp the NTSC video signal acquisition, processing, and realization method of the VGA display.

The following block diagram and the description of DE2_70_TV design as shown in Figure 5 are taken from Altera's DE2_70 User Manual.

Figure 5 shows the block diagram of the design. There are two major blocks in the circuit, called I2C_AV_Config and TV_to_VGA. The TV_to_VGA block consists of the ITU-R 656 Decoder, SDRAM Frame Buffer, YUV422 to YUV444, YCrCb to RGB, and VGA Controller. This figure also shows the TV Decoder (ADV7181) and the VGA DAC (ADV7123) chips used.

As soon as the bit stream is downloaded into the FPGA, the register values of the TV Decoder chip are used to configure the TV decoder via the I2C_AV_Config block, which uses the I2C protocol to communicate with the TV Decoder chip. Following the power-on sequence, the TV Decoder chip will be unstable for a time period; the Lock Detector is responsible for detecting this state.

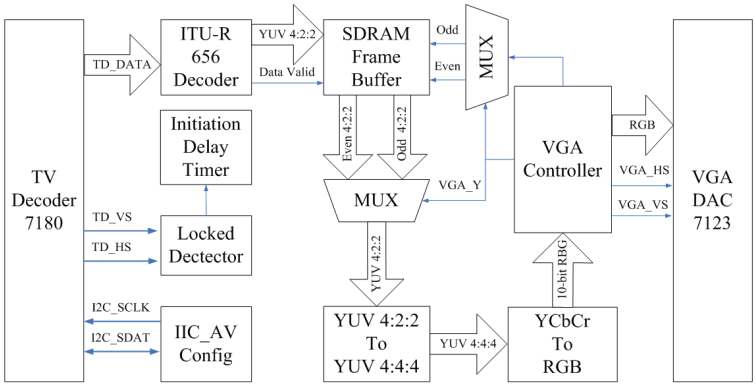


*Figure 5. The block diagram design of one-channel*

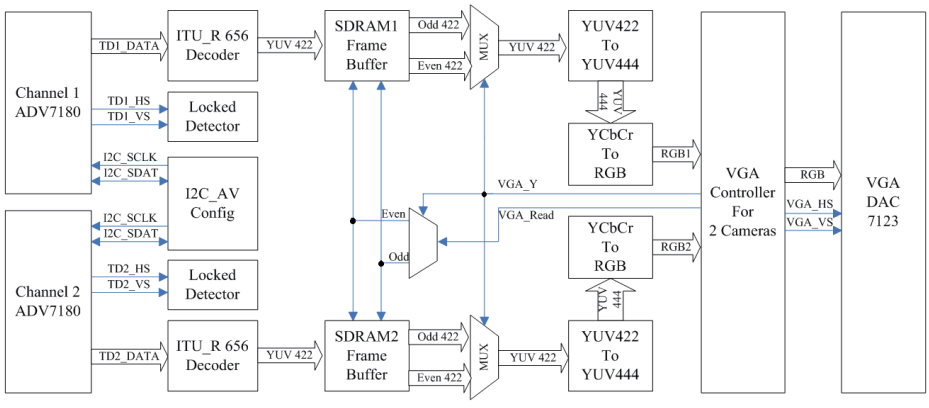


*Figure 6. The design schemes of two-channel*

The ITU-R 656 Decoder block extracts YCrCb 4:2:2 (YUV 4:2:2) video signals from the ITU-R 656 data stream sent from the TV Decoder. It also generates a valid control signal indicating the valid period of data output. Because the video signal from the TV Decoder is interlaced, we need to perform de-interlacing on the data source. We use the SDRAM Frame Buffer and a field selection multiplexer (MUX) which is controlled by the VGA controller to perform the de-interlacing operation. Internally, the VGA Controller generates data request and odd/even selected signals to the SDRAM Frame Buffer and filed selection multiplexer (MUX). The YUV422 to YUV444 block converts the selected YCrCb 4:2:2 (YUV 4:2:2) video data to the YCrCb 4:4:4 (YUV 4:4:4) video data format.

Finally, the YCrCb_to_RGB block converts the YCrCb data into RGB output. The VGA Controller block generates standard VGA sync signals VGA_HS and VGA_VS to enable the display on a VGA monitor. For more detailed information, please refer to Altera's DE2-70 User Manual.

2) Similar to the DE2_70_TV example, we can realize the acquisition, processing and the VGA synchronous display for 2-channel video signal. The design schemes are detailed in Figure 6.

Different from DE2_70_TV example, proposed work uses the same clock to read video data from 2 pieces SDRAM Frame Buffer synchronously, modifies the VGA logical display, and realizes single-channel video display, switch and synthetic display.

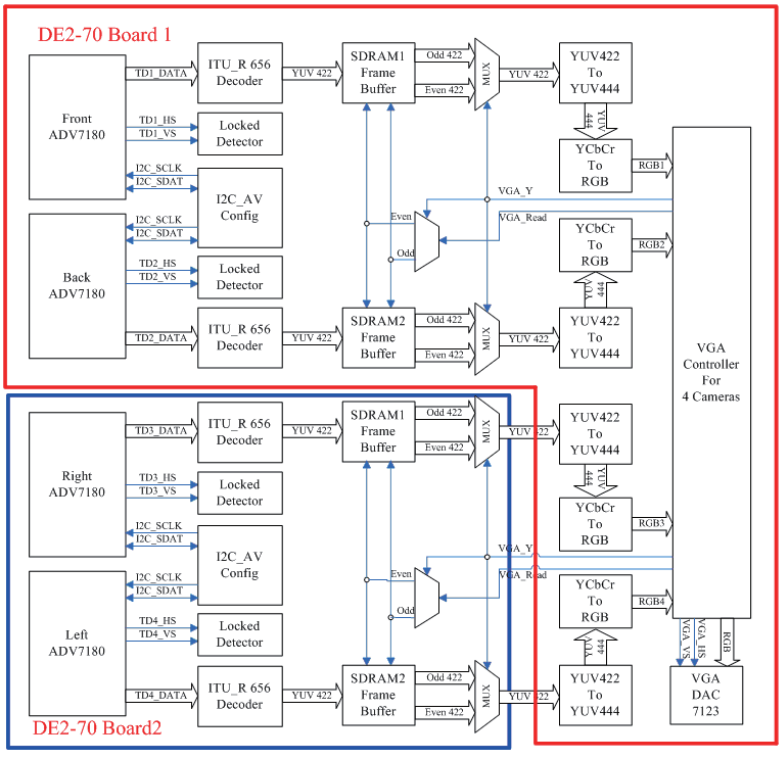


*Figure 7. The design schemes of four-channel*

3) Using the two pieces of DE2-70 development boards, we can realize the acquisition, processing and the VGA synchronous display for the 4-channel video signal. An implementation block diagram is shown in Figure7.

Unlike the 2-channel video signal processing, the 4-channel video signal processing uses the extended GPIO port to transport synchronous control signal and video data between two pieces of DE2-70 development boards.

4) 3D video source synthesis. In order to synthetize 3D video source, you need to arrange the four-channel pictures into cross-shaped on VGA monitor. Specific display area is shown in Figure8:

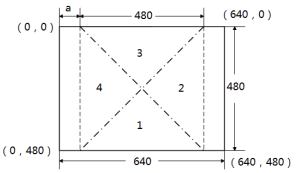


*Figure 8. Area partition*

The relationship between the pixel coordinates of the respective areas is as follows:

```
Parameter  a = 80;
Parameter  b = a+480;
if ((oCurrent_X < a ) | | (oCurrent_X > b )) //Blank area
else if ( oCurrent_Y>oCurrent_X-a )  // 1 area or 4 area
          begin
            if ( oCurrent_Y+oCurrent_X> b ) // 1 area
            else                            // 4 area
end
else   // 2 area or 3 area
          begin
            if ( oCurrent_Y+oCurrent_X> b ) // 2 area
            else                            // 3 area
          end
```

VGA output data can flexibly switch between the 4-channel video source data in terms of the position of the pixel coordinates.

5) Background eraser algorithm. In order to achieve a better display, we introduce a simple background eraser algorithm. The specific method is: pre-shoot a background in SDRAM Frame Buffer, make the XOR calculation for background and video data capurted in real time, and control the display output threshold in order to eliminate environmental interference.

6) The synthesized image is projected onto a pyramid imaging. In the process of pyramid production, we have tried plexiglass and see-though membrane materials. In the actual test, each side of the plexiglass has a certain thickness, resulting in the imaging ghosting. Eventually we chose see-though membrane material to produce pyramid in order to achieve a better display effect.

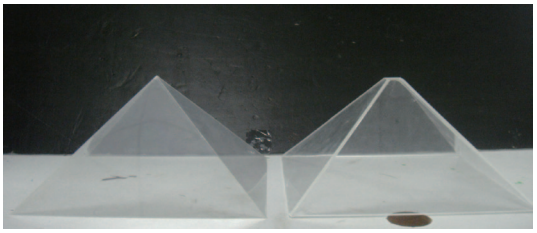

*Figure 9. See-though material*

## V. DESIGN FEATURES

The involved features of the proposed work mainly include:

### A. Camera Array

In order to truly represent 3D objects, the proposed work designs a camera array structure, taking pictures from the four directions around the same object, and then providing the signal source for the follow-up image synthesis algorithm.

### B. The hardware implementation of image processing algorithms

To ensure the stability, trueness and smoothness of the 3D effect, the proposed works realize

module of image processing algorithms with the hardware description language.

### C. Rectangular Pyramid Display Medium

Based on the principle of optical imaging, the proposed works break the shackles of the traditional 2D flat panel display medium and succeed in making the rectangular pyramid display medium, and resorting to the see-though material (computer the Screensavers film). Audiences are able to see images synthesized from each side of the four-sided pyramid, and enjoy the true 3D stereo effect without any auxiliary means (such as 3D glasses).

### D. SD Card Browser

In order to easily show, the proposed work has the picture browsing function with SD card. 3D video source files stored in the SD card can be played .

## CONCLUSION

The present solution scheme is based on FPGA design using SOPC technology, realizing the image processing and display, and SD card picture browsing function. Because of the high requirements of the real-time processing, the image information acquisition, processing, buffer and display are realized not by software but by hardware circuit module. NIOS II processor is responsible for sending various commands in order to control a variety of peripherals and to coordinate the work between different modules. Combining innovative thinking of SOPC design with the use of NIOS II processor, our works improve the flexibility of the design of system control, reduce the design burden. Hence, a platform could be built more rapidly based on the present solution scheme.

NIOS soft-core processor is an innovative idea for embedded system design. After a few months of practice, we fully appreciate the NIOS soft-core processor as a powerful embedded processor. In the SOPC Builder design system, the user can customize system components in accordance with the system requirements, while the development tools provide many of the most common IP cores for users to directly call. In addition, it also allows users to add custom peripherals in order to simply system hardware design. As a result, we can concentrate on the system function development and algorithm design, which greatly benefits to increase the efficiency of system design .

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